RN SHETTY TRUST ®

RNS INSTITUTE OF TECHNOLOGY

Autonomous Institution affiliated to Visvesvaraya Technological University, Belagavi
Approved By AICTE, New Delhi. Accredited by NAAC 'A+' Grade
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Dr. R N Shetty
Founder

ESTD.: 2001
An Institute with a Difference



DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

BACHELOR OF ENGINEERING

Scheme and Syllabus of III & IV Semesters

2025 SCHEME

www.rnsit.ac.in

ESTD.: 2001

An Institute with a Difference

Scheme and Syllabus
Batch 2025 – 2029

3rd and 4th Semester

(As per NEP - 2020)

(Effective from the academic year 2025 – 26)

ESTD : 2001
An Institute with a Difference

RNSIT

RNSIT (RNS Institute of Technology)

RNS Institute of Technology, familiar as RNSIT was established in the year 2001. It is the brainchild of Dr. R. N. Shetty, well known industrialist, and a great philanthropist. The institution was established with a sole purpose of imparting quality education in Engineering, Technology and Management. Being one of the premier engineering colleges in the country RNSIT is marching towards placing itself in the global map by excelling in academics and placements. Lush green campus, state of the art infrastructure, well equipped laboratories, hundreds of activities, numerous new initiatives, consistent VTU ranks, path breaking placements, cultural extravaganza, Sports events, 5600 + students and 300 + faculty – with all these RNSIT has become dream destination for engineering aspirants across the country.

Vision

Building RNSIT into a World Class Institution

Mission

To impart high-quality education in Engineering, Technology and Management with a difference, enabling students to excel in their career by

- Attracting quality Students and preparing them with a strong foundation in fundamentals so as to achieve distinctions in various walks of life leading to outstanding contributions
- Imparting value based, need based, choice based and skill based professional education to the aspiring youth and carving them into disciplined, World class Professionals with social responsibility
- Promoting excellence in Teaching, Research and Consultancy that galvanizes academic consciousness among Faculty and Students
- Exposing Students to emerging frontiers of knowledge in various domains and make them suitable for Industry, Entrepreneurship, Higher studies, and Research and Development
- Providing freedom of action and choice for all the Stakeholders with better visibility

ECE (Electronics and Communication Engineering)

The department of Electronics and Communication Engineering was started in 2001 and is currently running BE and Research programs. The Department has well qualified, committed and experienced Faculty members, in various domains of ECE, like Communication, Signal Processing, Image Processing, VLSI, Optical Communication, Antenna Design. The course covers the fundamental theoretical aspects as well as design level topics of all the above areas. The department has well structural labs to give students a practical exposure in the field of Analog Electronics, Analog Communication, Digital Signal Processing, Embedded Systems, Antennas and VLSI.

Vision

Conquering technical frontiers in the field of Electronics and Communication

Mission

The Department of Electronics and communication Engineering promotes an intellectual and ethical environment in which the strengths and skills of Electronics Professionals will flourish by:

- Achieving and fostering excellence in core Electronics and Communication engineering with focus on hardware, simulation and design.
- Pursuing Research, development and consultancy to achieve self-sustenance.
- Preparing industry ready graduates by providing skill training and nurturing innovation and creativity.

Programme Educational objectives (PEOs)

ECE Graduates, within three-five years of graduation should be able to:

- **PEO1:** Apply fundamental concepts obtained from mathematics, basic sciences and engineering subjects to solve challenging problems in Electronics, Communication and allied disciplines.
- **PEO2:** Exhibit technical and analytical skills for the design and development of innovative and cost-effective solutions.
- **PEO3:** Pursue higher education and participate in Lifelong learning to emerge as good human beings and responsible citizens.
- **PEO4:** Adapt to rapid changes in tools and technology and work in multidisciplinary fields to come up with new sustainable technologies catering to societal needs.

- **PEO5:** Cultivate skills which helps in building leadership qualities, entrepreneurships, effective communication and ethics needed for a successful professional career.

Program Outcomes (Revised)

- **PO1: Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization as specified in WK1 to WK4 respectively to develop to the solution of complex engineering problems.
- **PO2: Problem Analysis:** Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions with consideration for sustainable development. (WK1 to WK2).
- **PO3: Design/Development of solutions:** Design creative solutions for complex engineering problems and design/develop system/components or processes to meet the identified needs with consideration for the public health and safety, whole – life cost, net zero carbon, culture, society and environment as required. (WK5)
- **PO4: Conduct Investigations of Complex Problems:** Conduct investigation of complex engineering problems using research – based knowledge including design of experiments, modelling, analysis & interpretation of data to provide valid conclusions. (WK8)
- **PO5: Engineering tool usage:** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling recognizing their limitations to solve complex engineering problems. (WK2 and WK6)
- **PO6: The engineer and world:** Analyze and evaluate societal and environmental aspects while solving complex engineering problems for its impact on sustainability with reference to economy, health, safety, legal framework, culture and environment.
- **PO7: Ethics:** Apply ethical principles and commit to professional ethics, human values, diversity and inclusion; adhere to national and international laws. (WK9)
- **PO8: Individual and Collaborative Teamwork:** Function effectively as an individual, and as a member or leader in diverse/multi – disciplinary teams.
- **PO9: Communication:** Communicate effectively and inclusively within the engineering community and society at large, such as being able to comprehend and write effective reports and design documentation, make effective presentation considering cultural, language, and learning differences.
- **PO10: Project management and finance:** Apply knowledge and understanding of engineering management principles and economic decision – making and apply these to one's own work, as a member and leader in a team, and to manage projects and in multidisciplinary environments.

- **PO11: Life-long learning:** Recognize the need for and have the preparation and ability i) independent and life – long learning

  ii) adaptability to new and emerging technologies and

  iii) critical thinking in the broadest context of technological change. (WK8)

Program Specific Outcomes (PSOs)

The graduates of the department will be able to:

- **PSO1:** Apply knowledge of Electronic circuits and Communication systems in the design, development and analysis of integrated electronic systems to enhance human life.
- **PSO2:** Demonstrate competence in using Modern hardware languages, IT tools and create innovative electronic technologies as per industry standards.

ESTD : 2001
An Institute with a Difference

BE in Electronics and Communication Engineering (Autonomous Scheme – 2025)
3rd Semester

Sl. No.	Course	Course Code	Course Title	TD/PSB	Teaching & Learning Scheme					Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Practical (P)	(TW+SL) /Sem	TH/S	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	ASC	25BECTH301	Transform Techniques and Probability Distributions	TD /PSB: Mathematics / ECE Allied	45	30	0	45	120	3	50	50	100	4
2	IPCC	25BECIC302	Digital Systems Design using Verilog	ECE	45	0	30	45	120	3	50	50	100	4
3	PCC	25BECTH303	Network Analysis	ECE	45	30	0	45	120	3	50	50	100	4
4	PCC	25BECTH304	Analog Electronic Circuits	ECE	45	0	0	45	90	3	50	50	100	3
5	PCC	25BECTH305	Signals and Systems	ECE	45	0	0	45	90	3	50	50	100	3
6	PCCL	25BECLB306	Analog and Digital Electronics Lab	ECE	0	0	30	0	30	3	50	50	100	1
7	AEC	25BECAE307X	Ability Enhancement Course (BUCKET LIST - E)	ECE	0	0	30	0	30	3	50	50	100	1
8	SDC	25BCBPR308	Community Project (Project-Based Learning) / Societal Project	Respective Engineering Dept.	0	0	0	30	30	3	50	50	100	1
9	NCMC	25BNSSP309	National Service Scheme (NSS)	NSS coordinator	0	0	0	30	30	-	100	-	100	PP
		25BPEDU309	Physical Education (PE) (Sports and Athletics)	Physical Education Director										
		25BYOGA309	Yoga	Yoga Teacher										
		25BMUSK309	Music	Music Teacher										
				Total							**500**	**400**	**900**	**21**
10	NCMC	25BMADP310	Mathematics course for Lateral Entry Students	TD -Maths Dept	14	0	0	14	28	3	100	-	100	PP
				Total					**688**		**600**	**400**	**1000**	**21**
	NOTE: I SEMESTER CHEMISTRY CYCLE SECTIONS WILL STUDY "ENVIRONMENTAL STUDIES" IN IV SEMESTER AND "BIOLOGY FOR ENGINEERS" IN V SEMESTER													

NOTE: I SEMESTER PHYSICS CYCLE SECTIONS WILL STUDY "BIOLOGY FOR ENGINEERS" IN IV SEMESTER AND "ENVIRONMENTAL STUDIES" IN V SEMESTER

Sl. No.	Course	Course Code	Course Title	TD/PSB	Teaching & Learning Scheme					Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Practical (P)	(TW+SL) /Sem	# TH/S	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
11	SKLAB	25BECSL00X	SKILL LAB (BUCKET LIST - F)	ECE	0	0	30	0	30	3	50	50	100	1
NOTE: IN SEMESTER III, 50% OF THE STUDENTS WILL STUDY **"VLSI AND EMBEDDED SYSTEMS"** AND THE REMAINING 50% WILL STUDY **"SIGNAL PROCESSING APPLICATIONS WITH AI"**. IN SEMESTER IV, THE COURSES WILL BE INTERCHANGED BETWEEN THE TWO GROUPS.														

(BUCKET LIST - E) - PROFESSIONAL ELECTIVE COURSE – BEC515X		
Sl. No	**COURSE CODE**	**COURSE TITLE**
1	25BECAE307A	IoT Lab
2	25BECAE307B	Data Structures using C Lab
3	25BECAE307C	Circuits Simulation Lab
4	25BECAE307D	Signals and Systems Lab

(BUCKET LIST - F) – SKILL LAB – BECSL00X		
Sl. No	**COURSE CODE**	**COURSE TITLE**
1	25BECSL001	VLSI and Embedded System
2	25BECSL002	Signal Processing Applications with AI

BE in Electronics and Communication Engineering (Autonomous Scheme – 2025)

4th Semester

Sl. No.	Course	Course Code	Course Title	TD/PSB	Teaching & Learning Scheme					Examination				Credits
					Theory Lecture (L)	Tutorial (T)	Practical (P)	(TW+SL) /Sem	# TH/S	Duration in Hours	CIE Marks	SEE Marks	Total Marks	
1	ASC	25BECTH401	Mathematics for Machine Learning	TD: CS Allied/Maths PSB:CS Allied	45	30	0	45	120	3	50	50	100	4
2	IPCC	25BECIC402	Digital Signal Processing	ECE	45	0	30	45	120	3	50	50	100	4
3	PCC	25BECTH403	Communication Systems	ECE	45	30	0	45	120	3	50	50	100	4
4	PCC	25BECTH404	Control Systems	ECE	45	30	0	45	120	3	50	50	100	4
5	PCCL	25BECLB405	Communication Lab	ECE	0	0	30	00	30	**3**	50	50	100	1
6	AEC	25BECAE406X	Ability Enhancement Course (Laboratory) (BUCKET LIST - H)	ECE	0	0	30	00	30	3	50	50	100	1
7	BSC	25BFETH407	Biology for Engineers	TD: Chemistry/Biotech/ECE Allied; PSB: ECE Allied	30	0	0	30	60	2	50	50	100	2
8	SDC	25BESPR408	Environmental Science Project	Respective Engineering Dept.	0	0	0	30	30	3	50	50	100	1
9	NCMC	25BNSSP409	National Service Scheme (NSS)	NSS coordinator	0	0	0	30	30	--	100	--	100	PP
		25BPEDU409	Physical Education (PE) (Sports and Athletics)	Physical Education Director										

		25BYOGA409	Yoga	Yoga Teacher										
		25BMUSK409	Music	Music Teacher										
				Total					**660**		**500**	**400**	**900**	**21**
10	NCMC	25BMADP410	Mathematics course for Lateral Entry Students	TD -Maths Dept	14	0	0	14	28	--	100	--	100	PP
Total									**688**		**600**	**400**	**1000**	**21**
11	SKLAB	25BECSL00X	SKILL LAB (BUCKET LIST - F)	ECE	0	0	30	0	30	3	50	50	100	1
NOTE: IN SEMESTER III, 50% OF THE STUDENTS WILL STUDY **"VLSI AND EMBEDDED SYSTEMS"** AND THE REMAINING 50% WILL STUDY **"SIGNAL PROCESSING APPLICATIONS WITH AI"**. IN SEMESTER IV, THE COURSES WILL BE INTERCHANGED BETWEEN THE TWO GROUPS.														

(BUCKET LIST - H) – ABILITY ENHANCEMENT COURSE OR SKILL ENHANCEMENT COURSE - BECT657X / BECL657X		
Sl. No	**COURSE CODE**	**COURSE TITLE**
1	25BECAE406A	Machine Learning Lab
2	25BECAE406B	Control Systems Lab
3	25BECAE406C	FPGA Based Systems lab
4	25BECAE406D	Graphical Programming using LabView

(BUCKET LIST - F) – SKILL LAB – BECSL00X		
Sl. No	**COURSE CODE**	**COURSE TITLE**
1	25BECSL001	VLSI and Embedded System
2	25BECSL002	Signal Processing Applications with AI

III SEMESTER COURSES

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B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – III			
Course Title	**Transform Techniques and Probability Distributions**		
Course Code	**25BECTH301**	**CIE Marks**	**50**
(L: T: P) + SL	**(45: 30: 0) + 45 Hours / Sem**	**SEE Marks**	**50**
Credits	**4**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Learn to use Fourier series to represent periodical physical phenomena in engineering analysis.
- Apply Fourier transforms techniques to transform functions from time domain to frequency domain and vice versa.
- Apply Z transforms to solve difference equations.
- Develop the knowledge of probability laws and distribution of discrete and continuous random variables.

Module-1	**Fourier series**	**9 hrs**

Periodic functions, Dirichlet's condition. Importance of Fourier Series. Fourier series expansion of functions with period 2π and with arbitrary period: Rectangular wave, Half-wave rectifier, rectangular pulse, Saw tooth wave. A word on Vector spaces. Half-range Fourier series. Practical harmonic analysis, variation of periodic current. Complex Fourier series. Limitations of Fourier Series.

Module-2	**Fourier Transforms**	**9 hrs**

Importance of Fourier Transforms. Fourier Transforms from Fourier series - discussion. Fourier transforms, Fourier cosine and sine transforms, Inverse Fourier transforms, Inverse Fourier cosine and sine transforms. Fourier Transform from Fourier Series. Introduction to Discrete Fourier transform (DFT). Discussion of Limitations of Fourier Transforms and necessity of Wavelet Transforms.

Module-3	**Z Transforms**	**9 hrs**

Definition, Z-transforms of basic sequences and standard functions. Properties: Linearity, scaling, damping and shifting. Initial and final value theorems. Inverse Z- transforms. Application to solve difference equations.

Module-4	**Introduction to Probability**	**9 hrs**

Probability of an event, empirical and axiomatic definition, probability associated with set theory, addition law, conditional probability, multiplication law, Bayes' theorem. Application: Naive Bayes classifier.

Module-5	Probability Distributions	9 hrs
Random variables (discrete and continuous), probability mass/density function, Binomial distribution, Poisson distribution, exponential distribution and normal distribution. (Derivation of Mean and Standard Deviation for Binomial and Poisson distributions only)		

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Apply Fourier series techniques to express periodic waveforms—such as rectangular, sawtooth, and half-wave rectified signals—in both standard and half-range functional domains.
CO2	Determine the Fourier, sine, and cosine transforms (and their inverses) for continuous signals, and compute discrete Fourier transforms (DFT) for digital signal representations.
CO3	Solve linear difference equations by applying the properties, theorems, and inverse operations of the Z-transform to discrete-time sequences.
CO4	Calculate probabilistic relationships among events and evaluate classification outcomes using the Naïve Bayes algorithm.
CO5	Determine real-world probabilistic scenarios by categorizing random variables and executing calculations using Binomial, Poisson, and exponential probability distributions.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	30	-	Two tests each of 50 marks shall be conducted. Average of Two Internal Assessment Tests shall be scaled down to 30 marks.
Continuous and Comprehensive Evaluation (B)	20	-	Any two Assessment methods as per 24RNBE4.2 (*if it is project based, one assignment shall be given), scaled to 20 marks.
Total CIE (A+B)	**50**	**20**	**CIE Evaluation is done for a maximum of 50 marks**
SEE (C)	**50**	**18**	**SEE is a theory exam conducted for 100 marks and scaled down to 50 marks. Exam duration shall be for 3 hours.**

CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

Text Books:

1.	B. S. Grewal, "Higher Engineering Mathematics", Khanna Publishers, 44th Ed., 2021
2.	E. Kreyszig, "Advanced Engineering Mathematics", John Wiley & Sons, 10th Ed., 2018

Reference Books:

1.	B.V. Ramana, "Higher Engineering Mathematics" McGraw-Hill Education, 11thEd., 2017
2.	N.P Bali and Manish Goyal, "A Textbook of Engineering Mathematics" Laxmi Publications, 10th Ed., 2022
3.	H.K. Dass and Er. Rajnish Verma, "Higher Engineering Mathematics" S. Chand Publication, 3rd Ed., 2014

Weblinks and Video Lectures:

1.	https://onlinecourses.nptel.ac.in/e-learning/preview/noc26_ma120
2.	https://onlinecourses.nptel.ac.in/e-learning/preview/noc26_ma107

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B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – III			
Course Title	**Digital System Design using Verilog**		
Course Code	**25BECIC302**	**CIE Marks**	**50**
(L: T: P) + SL	**(45: 0: 30) + 45 Hours / sem**	**SEE Marks**	**50**
Credits	**4**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- To impart the concepts of simplifying Boolean expression using K-map techniques and Quine-McCluskey minimization techniques.
- To impart the concepts of designing and analyzing combinational logic circuits.
- To impart design methods and analysis of sequential logic circuits.
- To impart the concepts of Verilog HDL-data flow and behavioural models for the design of digital systems.

Module-1	**Principles of Combinational Logic**	**9 hrs**

Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables, Karnaugh maps-up to 4 variables, Quine-McCluskey Minimization Technique. Quine-McCluskey using Don't Care Terms. **(Section 3.1 to 3.5 of Text1).**

Module-2	**Logic Design with MSI Components and Programmable Logic Devices**	**9 hrs**

Binary Adders and Subtractors, Decoders, Multiplexers, Programmable Logic Devices (PLDs), **(Section 5.1,5.2,5.4.5.6.5.7 of Text 2)**

Field Programmable Gate Arrays, Xilinx FPGA (only introduction) (Section 9.6,9.61 of Text1)

Self-study component: Comparators, Encoders (5.3, 5.5 of Text 2).

Module-3	**Flip-Flops and its Applications**	**9 hrs**

The Master-Slave Flip-flops (Pulse-Triggered flip-flops):SR flip-flops, JK flip flops, Characteristic equations, Registers, Binary Ripple Counters, Synchronous Binary Counters, Counters based on Shift Registers, Design of Synchronous mod-n Counter using clocked T, J K, D and SR flip-flops. (Section 6.4, 6.6 to 6.9 (Excluding 6.9.3) of Text2)

Synchronous Sequential Networks: Structure and Operation of Clocked Synchronous Sequential Networks. (Section 7, 7.1 of Text 2)

Module-4	**Introduction to Verilog**	**9 hrs**

Introduction to Verilog: Structure of Verilog module, Operators, Data Types, Styles of Description. (Section 1.1 to 1.6.2, 1.6.4 (only Verilog) of Text3))

Verilog Data flow description: Highlights of Data flow description, Structure of Data flow description. (Section 2.1 to 2.2(only Verilog) of Text3) **Verilog Structural description:** Highlights of Structural description, Organization of structural description, Structural description of ripple carry adder. (Section 4.1 to 4.2 of Text 3)		
Module-5	**Verilog Behavioural description**	**9 hrs**
Verilog Behavioural description: Structure, Variable Assignment Statement, Sequential Statements, Loop Statements, Verilog Behavioural Description of Multiplexers (2:1, 4:1, 8:1). (Section 3.1 to 3.4 (only Verilog) of Text 3) **Behavioural Modelling:** Structured procedures, Structured assignment (7 ,7.1&7.2 of Text 4)		

Practical component of IPCC:

Experiments can be conducted either using any circuit simulation software or discrete components (but not limited to):

Exp. No.	Programs
1	To simplify the given Boolean expressions and realize using Verilog program
2	To realize Adder/Subtractor (Full/half) circuits using Verilog data flow description.
3	To realize 4-bit ALU using the Verilog program.
4	To realize the following Code converters using Verilog Behavioral description a) Gray to binary and vice versa b) Binary to excess-3 and vice versa
5	To realize using Verilog Behavioral description: 8:1mux, 8:3encoder, Priority encoder
6	To realize using Verilog Behavioral description: 1:8Demux, 3:8 decoder,2 –bit Comparator
7	To realize using Verilog Behavioral description: Flip-flops: a)JK type b) SR type c) T type d) D type
8	To realize Counters-up/down (BCD and binary) using Verilog Behavioral description.
Demonstration Experiments (For CIE only–not to be included for SEE) Use FPGA/CPLD kits for downloading Verilog codes and check the output for interfacing experiments.	
9	Verilog Program to interface a Stepper motor to the FPGA/CPLD and rotate the motor in the specified direction (by N steps).
10	Verilog programs to interface Switches and LEDs to the FPGA/CPLD and demonstrate its working.

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Simplify Boolean functions using K-map and Quine-McCluskey minimization techniques.
CO2	Analyze and design for combinational logic circuits
CO3	Analyze the concepts of Flip Flops (SR, D, T and JK) and to design the synchronous sequential circuits using Flip Flops.
CO4	Model Combinational circuits (adders, subtractors, multiplexers) and sequential circuits using Verilog descriptions.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE- IA Tests (A)	20	-	Two tests each of 50 marks shall be conducted. Average of Two Internal Assessment Tests shall be scaled down to 20 marks.
Continuous and Comprehensive Evaluation (B)	10	-	Any one Assessment method as per 24RNBE4.2 scaled to 10 marks.
Total CIE Theory (A+B)	**30**	**12**	**Marks of Tests and Assignments awarded for a maximum of 30.**
CIE Practical	12	-	Marks awarded for Weekly Conduction of Experiments and Submission of Laboratory records, scaled to 12 marks.
CIE Practical Test	8	-	Average of marks of Two tests, each conducted for 100 marks covering all experiments, scaled to 8.
Total CIE Practical (C)	**20**	**8**	**Marks of Experiments, Record and Test awarded for a maximum of 20 marks.**
CIE: Theory + Practical (A+B+C)	**50**	**20**	**CIE Evaluation is done for a maximum of 50 marks.**
SEE (D)	**50**	**18**	**SEE is a theory exam, conducted for 100 marks and scaled down to 50 marks. Exam duration shall before 3 hours.**

CIE+SEE (A+B+C+D)	**100**	**40**	**Final marks shall be the sum of marks scored in Components A, B, C and D**

- The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included in their respective modules only.

Text Books:

1.	Digital Logic Applications and Design by John M Yarbrough, Thomson Learning,2001.
2.	Digital Principles and Design by Donald D Givone, Mc Graw Hill, 2002.
3.	HDL Programming VHDL and Verilog by Nazeih M Botros, 2009 reprint, Dream tech press.
4.	Verilog HDL: A Guide to Digital Design and Synthesis “, Samir Palnitkar, Sun soft Express, 1996.

Reference Books:

1.	Fundamentals of logic design, by Charles H Roth Jr., Cengage Learning
2.	Logic Design, by Sudhakar Samuel, Pearson/Sanguine, 2007
3.	Fundamentals of HDL, by Cyril PR, Pearson/Sanguine, 2010

Weblinks and Video Lectures (e-Resources):

1.	https://nptel.ac.in/courses/106105185
2.	https://nptel.ac.in/courses/108103179

B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – III			
Course Title	**Network Analysis**		
Course Code	**24BECTH303**	**CIE Marks**	**50**
(L: T: P) + SL	**(45: 30: 0) + 45 Hours / Sem**	**SEE Marks**	**50**
Credits	**4**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Understand the fundamental concepts of circuit analysis
- Understand the conclusions of Network theorems
- Understand the concept of Initial and final conditions and their use in finding total response.
- Understand the circuit analysis techniques using Laplace transform
- Determine two-port network parameters
- Determine the resonant frequency, bandwidth and quality factor of resonant circuits.

Prerequisites: Ohm's law, Kirchhoff's laws, Laplace transform definition and properties

Module-1	**Fundamental Circuit Concepts**	**9 hrs**

Ideal and Practical sources, source transformation, mesh analysis of the networks consisting independent and dependent DC/AC sources, concept of supermesh, node analysis of the networks consisting independent and dependent DC/AC sources, concept of supernode, source shifting, star-delta transformations

Module-2	**Network Theorems**	**9 hrs**

Superposition theorem, Thevenin's theorem, Norton's theorem, Maximum power transfer theorem, Reciprocity theorem, Millman's theorem, Miller's theorem

Module-3	**Initial conditions and Solutions of networks excited by DC source**	**9 hrs**

Introduction to Initial conditions and Why study them? Representation of R, L and C elements under initial and final conditions, Evaluation of initial and final conditions of DC and AC excited networks, Solution of DC source excited networks (RL, RC, RLC) characterized by Differential equations

Module-4	**Applications of Laplace Transform**	**9 hrs**

Introduction to standard test signals (step, impulse, ramp and sinusoidal) and derivation of their Laplace transforms, Laplace transforms of periodic waveforms (square, triangular, sawtooth, etc.), Laplace transform properties: Convolution theorem, Initial and Final value theorems, Solution of

networks using Laplace transform, Transfer function, Derivation of transfer functions of circuits involving R, L, and C elements.		
Module-5	**Two-port Networks and Resonant circuits**	**9 hrs**
Two-port network introduction, Z-parameters, Y-parameters, ABCD parameters and h-parameters, Relationship between parameter sets. Resonant circuits: Series and Parallel resonant circuits, resonant frequency, derivation of relationships between resonant frequency, bandwidth and Q-factor		

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Solve the network problems using mesh analysis, node analysis, source transformation, source shifting techniques, star-delta transformation and network theorems.
CO2	Evaluate initial and final conditions of the networks excited by DC and AC sources, and solve the differential equations to find the responses of RL, RC and RLC networks excited by DC source.
CO3	Apply the Laplace transform to solve the network problems and determine transfer functions.
CO4	Evaluate the network parameters of two-port networks and performance parameters of resonant circuits, such as resonant frequency, bandwidth and Q-factor.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	30	-	Two tests each of 50 marks shall be conducted. Average of Two Internal Assessment Tests shall be scaled down to 30 marks.
Continuous and Comprehensive Evaluation (B)	20	-	Any two Assessment methods as per 24RNBE4.2 (*if it is project based, one assignment shall be given), scaled to 20 marks.
Total CIE (A+B)	**50**	**20**	**CIE Evaluation is done for a maximum of 50 marks**
SEE (C)	**50**	**18**	**SEE is a theory exam conducted for 100 marks and scaled down to 50 marks. Exam duration shall be for 3 hours.**

CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

Text Books:

1.	D. Roy Choudhury, "Networks and Systems", 3rd Edition, New Age International Publishers, 2023
2.	M. E. Van Valkenburg and T S Rathore, "Network Analysis, Revised", 3rd Edition, Pearson India Publishers, 2019.

Reference Books:

1.	Jr H. William Hayt, Jack Kemmerly, Jamie Phillips and Steven Durbin, "Engineering Circuit Analysis", 10th Edition, Mc Graw Hill Indian Edition, 2024
2.	Joseph A Edminister and Mahmood Nahvi, "Electric Circuits (Schaum's Outlines Series)", 5th Edition, Mc Graw Hill Education, 2017

Weblinks and Video Lectures:

1.	https://nptel.ac.in/courses/108105159

ESTD : 2001
An Institute with a Difference

B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – III			
Course Title	**Analog Electronic Circuits**		
Course Code	**25BECTH304**	**CIE Marks**	**50**
(L: T: P) + SL	**(45: 0: 0) + 45 Hours / Sem**	**SEE Marks**	**50**
Credits	**3**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Understand the operation and characteristics of BJT and MOSFET devices.
- Analyze transistor amplifier circuits using appropriate small-signal models.
- Apply biasing techniques for stable operation of BJT and MOSFET amplifiers.
- Design and analyze linear and non-linear operational amplifier circuits for various applications.
- Study data converters, 555 timer circuits, and oscillator circuits used in analog electronic systems.

Module-1	**Bipolar Junction Transistors**	**9 hrs**

Small signal operations and models: The Collector Current and the Transconductance, The Base Current and the Input Resistance at the Base, The Emitter Current and the Input Resistance at the Emitter, Voltage Gain, The Hybrid-π Model, The T-Model, Application of the Small-Signal equivalent Circuit, Performing Small-Signal Analysis Directly on the Circuit Diagram, Augmenting the Small-Signal Models to Account for the Early effects.

Single-Stage BJT Amplifiers: The Basic Structure, Characterizing BJT Amplifiers, The Common-Emitter (CE) Amplifier, The Common-Emitter Amplifier with an Emitter Resistance, The Common-Base (CB) Amplifier, The Common-Collector (CC) Amplifier or Emitter Follower.

Text 1

Module-2	**MOS Field-Effect Transistors (MOSFETs)-1**	**9 hrs**

Device structure and physical operation: Device Structure, Operation with No Gate Voltage, Creating a channel for current flow, Applying a small v_{DS}, Operation as v_{DS} is increased, Derivation of the i_D-v_{DS} Relationship.

Current-Voltage Characteristics: Circuit Symbol, The i_D-v_{DS} Characteristics, Finite Output Resistance in Saturation.

MOSFET circuits at DC, MOSFET as an amplifier and as a switch: Large Signal Operation-Transfer Characteristics, Graphical and Analytical derivation of the Transfer characteristics.

Biasing in MOS amplifier circuits: Biasing by fixing V_{GS}, Biasing by fixing VG and connecting a source resistance, Biasing using a Drain-to-Gate feedback resistor, Biasing using constant Current source. **Text 1**

Module-3	MOS Field-Effect Transistors (MOSFETs)-2	9 hrs
Small Signal Operations and Models: DC bias point, Signal current in the Drain terminal, Voltage gain, Small-signal equivalent circuit models, Transconductance, The T equivalent circuit model. **Single-Stage MOS Amplifiers:** Basic structure, Characterising amplifiers, The Common-Source (CS) amplifier, The Common-Source amplifier with a Source resistance, The Common-Gate (CG) amplifier, The Common-Drain (CD) or Source-Follower amplifier. **Text 1**		
Module-4	**Linear Op-amps applications**	**9 hrs**
Summing, Scaling and Averaging amplifiers, Instrumentation Amplifier, Voltage to current converter with grounded load, Current to voltage converter: DAC using current to voltage converter, Practical Integrator and Differentiator. **Active filters:** First order Low-Pass Butterworth filter, Second order Low-Pass Butterworth filter, First order High-Pass Butterworth filter, Second order High-Pass Butterworth filter, Band-pass filters. **Text 2**		
Module-5	**Non-Linear Op-amps applications**	**9 hrs**
Comparator, Schmitt Trigger, D/A converter with binary weighted resistors, D/A converter with R and 2R resistors, Successive approximation A/D converter, Peak detector, Sample and Hold circuit. **555 Timers:** Monostable and Astable Multivibrator. **Text 2** **Oscillators:** Wein Bridge oscillator, Phase-shift Oscillator, LC-tuned Oscillator, Crystal Oscillator. **Text 1**		

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Apply the principles of BJT small-signal models to analyze the performance of single-stage transistor amplifiers and determine gain, input and output resistance.
CO2	Apply MOSFET device characteristics and biasing techniques to determine the operating point and analyze the behaviour of MOSFET amplifier circuits.
CO3	Analyze and evaluate the performance of single-stage MOSFET amplifiers using appropriate small-signal equivalent circuit models.
CO4	Apply operational amplifier principles to design and analyze linear circuits such as amplifiers, active filters, integrators, differentiators, and instrumentation amplifiers.
CO5	Analyze and implement non-linear op-amp circuits, data converters, 555 timer circuits, and oscillator circuits for specified applications.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	30	-	Two tests each of 50 marks shall be conducted. Average of Two Internal Assessment Tests shall be scaled down to 30 marks.
Continuous and Comprehensive Evaluation (B)	20	-	Any two Assessment methods as per 24RNBE4.2 (*if it is project based, one assignment shall be given), scaled to 20 marks.
Total CIE (A+B)	**50**	**20**	**CIE Evaluation is done for a maximum of 50 marks**
SEE (C)	**50**	**18**	**SEE is a theory exam conducted for 100 marks and scaled down to 50 marks. Exam duration shall be for 3 hours.**
CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

Text Books:

1.	Adel S. Sedra, Kenneth C. Smith, "Microelectronic Circuits-Theory and Applications", Fifth Edition, Oxford University Press, 2013.
2.	Ramakant A. Gayakwad, "Op-Amps and Linear Integrated Circuits", Fourth Edition, Pearson Education Inc.

Reference Books:

1.	Albert Malvino, David J Bates, "Electronic Principles", 7th Edition, Tata McGraw Hill, ISBN: 0-07-063424-6
2.	Robert L. Boylestad, Louis Nashalsky, "Electronic Devices and Circuit Theory", Ninth Edition, Pearson Education, ISBN: 978-81-317-0314-4

Weblinks and Video Lectures:

1.	https://onlinecourses.nptel.ac.in/e-learning/preview/noc26_ee135

2.	https://onlinecourses.nptel.ac.in/e-learning/preview/noc26_ee174

ESTD : 2001
An Institute with a Difference

B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – III			
Course Title	**Signals and Systems**		
Course Code	**25BECTH305**	**CIE Marks**	**50**
(L: T: P) + SL	**(45: 0: 0) + 45 Hours / Sem**	**SEE Marks**	**50**
Credits	**3**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Understand the basic concepts of signals and systems.
- Analyze linear time-invariant (LTI) systems using time-domain methods.
- Represent and analyze signals using Fourier Series and Fourier Transform techniques.
- Apply Z-transform techniques to analyze discrete-time systems and their properties.

Module-1	**Introduction and Classification of Signals**	**9 hrs**

Definition of signal, Classification of signals, Basic operations on signals: Amplitude scaling, addition, Multiplication, Differentiation, and Integration of signals. Time scaling, Time shift, and Time reversal.

Elementary signals: Exponential signals, Sinusoidal signals, Relation between sinusoidal and complex exponential signals, Exponentially damped sinusoidal signals, Step function, Impulse function, Ramp function.

Module-2	**System**	**9 hrs**

Definition of system, Systems viewed as interconnections of operations, Properties of systems: Stability, Memory, Causality, Invertibility, Time invariance, Linearity.

Time domain representation of LTI Systems-I: Introduction, Convolution Sum, Convolution sum evaluation procedure, Convolution Integral, Convolution integral evaluation procedure.

Module-3	**Time domain representation of LTI Systems-II**	**9 hrs**

Interconnections of LTI systems, Relations between LTI system properties and the impulse response: Memoryless, Causal, Stable, Invertible and deconvolution, Step response.

Fourier representation of Periodic Signal: Fourier Series and Discrete-time Fourier series - Introduction, representation, basic problems.

Module-4	**Fourier Representation of Nonperiodic Signals**	**9 hrs**

Fourier Transform and DTFT- Introduction, representation and basic problems.

Properties of Fourier Representations: Linearity and symmetry, Convolution, Differentiation and Integration, Time and frequency shift, scaling, Parseval Theorem, Problems on properties of Fourier representations.

Applications of Fourier Representations to Mixed Signal Classes: Introduction, Fourier transform representations of periodic signals, Convolution and multiplication with mixtures of periodic and non-periodic signals, Fourier transform representation of discrete-time signals.		
Module-5	**Z-Transform**	**9 hrs**
Introduction, The z-transform, Properties of Region of Convergence, Properties of Z-Transforms, Inverse z-Transform (Partial Fraction Method only). The transfer function, Causality and stability, Determining the frequency response from poles and zeros, The unilateral z-transform.		

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Apply signal operations to classify and represent continuous-time and discrete-time signals.
CO2	Analyze system properties such as linearity, causality, stability, and time invariance.
CO3	Evaluate the response and characteristics of LTI systems using time-domain analysis techniques.
CO4	Apply Fourier representations and their properties to analyze signals in the frequency domain.
CO5	Apply Z-transform techniques to analyze discrete-time signals and systems.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	30	-	Two tests each of 50 marks shall be conducted. Average of Two Internal Assessment Tests shall be scaled down to 30 marks.
Continuous and Comprehensive Evaluation (B)	20	-	Any two Assessment methods as per 24RNBE4.2 (*if it is project based, one assignment shall be given), scaled to 20 marks.
Total CIE (A+B)	**50**	**20**	**CIE Evaluation is done for a maximum of 50 marks**
SEE (C)	**50**	**18**	**SEE is a theory exam conducted for 100 marks and scaled down to 50 marks. Exam duration shall be for 3 hours.**

CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

Text Books:

1.	Simon Haykin and Barry Van Veen, "Signals and Systems", 2nd Edition, Wiley India, 2008, ISBN: 9971-51-239-4.

Reference Books:

1.	Michael Roberts, "Fundamentals of Signals & Systems", 2nd edition, Tata McGraw-Hill, 2010, ISBN: 978-0-07-070221-9.
2.	Alan V. Oppenheim, Alan S. Willsky, and S. Hamid Nawab, "Signals and Systems", 2nd Edition, PHI Learning Pvt. Ltd., New Delhi, India, 2009. ISBN: 978-8120312463.

Weblinks and Video Lectures:

1.	https://nptel.ac.in/courses/108104100

ESTD : 2001
An Institute with a Difference

B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – III			
Course Title	**Analog and Digital Electronics Lab**		
Course Code	**25BECLB306**	**CIE Marks**	**50**
L: T: P	**0: 0: 30**	**SEE Marks**	**50**
Credits	**1**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Design, analyze, and test analog electronic circuits using BJTs, MOSFETs, Op-Amps, and timer ICs.
- Investigate the performance characteristics of amplifiers, oscillators, active filters, and multivibrators through experimental validation.
- Design and implement digital logic circuits such as code converters, flip-flops, counters, and DACs.
- Develop practical skills in circuit implementation, testing, troubleshooting, and measurement using laboratory instruments.
- Interpret experimental results and compare them with theoretical predictions.

Sl. No	Experiments
	Part 1: Analog Circuits
1	Design and test the BJT common emitter voltage amplifier and determine the gain, frequency response, bandwidth, maximum signal handling capacity, figure of merit, input and output impedances.
2	Design and test BJT based: a) RC Phase shift Oscillator b) Colpitts Oscillator
3	Design and test the MOSFET common source amplifier and determine the gain-bandwidth product, input and output impedances.
4	Design and test the second order Active Filters and plot the frequency response: a) Low-pass filter b) High-pass filter
5	Design and test the following using 555 timers: a) Monostable Multivibrator b) Astable Multivibrator
6	Design 4-bit R-2R Op-Amp Digital to Analog Converter: a) By taking binary input from toggle switches b) By generating digital inputs from mod-16 counter

	Part 2: Digital Circuits
7	Design and test the following code converters: a) Binary to Gray converter and vice versa b) BCD to Excess-3 and vice versa
8	Design and test the following flip-flops (Use only NAND gates): a) JK Master-Slave flip-flop b) D flip-flop c) T flip-flop
9	Design and test Ring and Johnson Counters using IC7495 (4-bit shift register)
10	Design and test the following counters: a) Mod-N synchronous Up/Down counter using IC7476 JK flip-flop b) Mod-N counter using IC7490/7476 c) Design and test Synchronous Counter using IC74192

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Design and test BJT and MOSFET amplifier circuits and evaluate their gain, bandwidth, and impedance characteristics.
CO2	Design and analyze transistor-based oscillators, active filters, and timer circuits to verify their operating characteristics.
CO3	Design and implement Op-Amp-based digital-to-analog converters and validate their performance experimentally.
CO4	Design and test combinational digital circuits including code converters and logic implementations using standard ICs and logic gates.
CO5	Design and verify sequential digital circuits such as flip-flops, ring counters, Johnson counters, and synchronous/asynchronous counters using SSI/MSI devices.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – Practical (A)	30	-	Marks awarded for Weekly Conduction of Experiments and Submission of Laboratory records, scaled to 20 marks.
CIE Practical Test (B)	20	-	Test conducted for part A and part B, each carries 5 marks and final IA test conducted for 20 Marks

Total CIE (A+B)	**50**	**20**	**Sum of Marks of Experiments, Record and Test shall be CIE marks awarded for a maximum of 50.**
SEE (C)	**50**	**20**	**SEE is a lab exam conducted for 100 marks and scaled down to 50 marks. Exam duration shall be for 3 hours.**
CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

Text Books:

1.	Adel S. Sedra, Kenneth C. Smith, "Microelectronic Circuits-Theory and Applications", Fifth Edition, Oxford University Press, 2013.
2.	Ramakant A. Gayakwad, "Op-Amps and Linear Integrated Circuits", Fourth Edition, Pearson Education Inc.
3.	Donald D. Givone, "Digital Principles and Design", Indian Edition, Mc Graw Hill, 2016.

ESTD : 2001
An Institute with a Difference

B.E. (Electronics and Communication Engineering)
Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
SEMESTER – III

Course Title	**Internet of Things Lab**		
Course Code	**25BECAE307A**	**CIE Marks**	**50**
L: T: P	**0: 0: 30**	**SEE Marks**	**50**
Credits	**1**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- To impart necessary and practical knowledge of components of the Internet of Things
- To develop skills required to build real-life IoT-based projects

Sl. No	**Experiments**
1	a) To interface LED/Buzzer with Arduino /Raspberry Pi and write a program to 'turn ON' LED for 1 sec after every 2 seconds. b) To interface the Push button/Digital sensor (IR/LDR) with Arduino /Raspberry Pi and write a program to 'turn ON' LED when a push button is pressed or at sensor detection.
2	a) To interface the DHT11 sensor with Arduino/Raspberry Pi and write a program to print temperature and humidity readings. b) To interface OLED with Arduino/Raspberry Pi and write a program to print its temperature and humidity readings.
3	To interface the motor using a relay with Arduino /Raspberry Pi and write a program to 'turn ON' the motor when a push button is pressed.
4	a) Write an Arduino/Raspberry Pi program to interface the Soil Moisture Sensor. b) Write an Arduino/Raspberry Pi program to interface the LDR/Photo Sensor.
5	Write a program to interface an Ultrasonic Sensor with Arduino/Raspberry Pi.
6	Write a program on Arduino/Raspberry Pi to upload temperature and humidity data to thingspeak cloud.
7	Write a program on Arduino/Raspberry Pi to retrieve temperature and humidity data from thingspeak cloud.
8	Write a program to interface LED using Telegram App.
9	Write a program on Arduino/Raspberry Pi to publish temperature data to the MQTT broker.
10	Write a program to create a UDP server on Arduino/Raspberry Pi and respond with humidity data to the UDP client when requested.
11	Write a program to create a TCP server on Arduino/Raspberry Pi and respond with humidity data to the TCP client when requested.

12	Write a program on Arduino/Raspberry Pi to subscribe to the MQTT broker for temperature data and print it.

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Analyse Internet of Things and its hardware and software components.
CO2	Interface I/O devices, sensors & communication modules.
CO3	Remotely monitor data and control devices.
CO4	Develop real-life IoT-based projects.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	20	-	Marks awarded for Weekly Conduction of Experiments and Submission of Laboratory records, scaled to 20 marks.
CIE Practical Test + Mini Project (B)	10 + 20	-	Test conducted for part A and part B, each carries 5 marks and final IA test conducted for 20 Marks
Total CIE (A+B)	**50**	**20**	**Sum of Marks of Experiments, Record and Test shall be CIE marks awarded for a maximum of 50.**
SEE (C)	**50**	**20**	**SEE is a practical exam conducted for 100 marks and scaled down to 50 marks. Exam duration shall be for 3 hours.**
CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – III			
Course Title	**Data structures using C Lab**		
Course Code	**25BECAE307B**	**CIE Marks**	**50**
L: T: P	**0: 0: 30**	**SEE Marks**	**50**
Credits	**1**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Develop Proficiency in designing and implementing fundamental data structures.
- Learn various sorting and searching algorithms and analyse their time complexity.
- Understand algorithmic problem-solving techniques, including recursion.
- Explore advanced data structures like trees, graphs, and hash tables.
- Apply data structures and algorithms knowledge to solve real-world programming challenges efficiently.

Sl. No	Experiments
1	Write a C Program to create a student record structure to store, N records, each record having the structure shown below: USN, Student Name and Semester. Write necessary functions: a) To display all the records in the file. b) To search for a specific record based on the USN. In case the record is not found, suitable message should be displayed. Both the options in this case must be demonstrated. (Use pointer to structure for dynamic memory allocation)
2	Write a C Program to construct a stack of integers and to perform the following operations on it: a) Push b) Pop c) Display the program should print appropriate messages for stack overflow, stack underflow, and stack empty.
3	Write a C Program to simulate the working of a queue of integers using an array. Provide the following operations: a) Insert b) Delete c) Display
4	Write a C Program using dynamic variables and pointers to construct a stack of integers using singly linked list and to perform the following operations: a) Push b) Pop c) Display the program should print appropriate messages for stack overflow and stack empty.

5	Write a C Program to support the following operations on a doubly linked list where each node consists of integers: a) Create a doubly linked list by adding each node at the front. b) Insert a new node to the left of the node whose key value is read as an input c) Delete the node of a given data, if it is found, otherwise display appropriate message. Display the contents of the list.
6	Write a C Program to construct, a) Binary search tree of integers. b) To traverse the tree using all the methods i.e., inorder, preorder and postorder. c) To display the elements in the tree.
7	Write recursive C Programs for a) Searching an element on a given list of integers using the Binary Search method. b) Solving the Towers of Hanoi problem.
8	Write a C Program: a) Traversing a graph using the Breadth First Search (BFS) method. b) Checking whether a given graph is connected or not using the Depth First Search (DFS) method.
9	Design and develop a program in C that uses Hash Function H:K->L as H(K)=K mod m (reminder method) and implement hashing technique to map a given key K to the address space L. Resolve the collision (if any) using linear probing.
10	Implement minimum cost spanning tree algorithms using C Program. a) Kruskal's Algorithm b) Prim's Algorithm

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Explain the concepts of structures, pointers, dynamic memory allocation, and file handling used in data structure implementation.
CO2	Apply stack, queue, and linked list operations to develop programs for data storage and manipulation.
CO3	Apply recursion techniques to solve searching and problem-solving applications.
CO4	Apply tree and graph traversal algorithms to construct and manipulate Binary Search Trees and Graphs.
CO5	Apply hashing and minimum spanning tree algorithms to solve data retrieval and graph optimization problems.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	20	-	Marks awarded for Weekly Conduction of Experiments and Submission of Laboratory records, scaled to 20 marks.
CIE Practical Test + Mini Project (B)	10 + 20	-	Test conducted for part A and part B, each carries 5 marks and final IA test conducted for 20 Marks
Total CIE (A+B)	**50**	**20**	**Sum of Marks of Experiments, Record and Test shall be CIE marks awarded for a maximum of 50.**
SEE (C)	**50**	**20**	**SEE is a lab exam conducted for 100 marks and scaled down to 50 marks. Exam duration shall be for 3 hours.**
CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

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B.E. (Electronics and Communication Engineering)
Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
SEMESTER – III

Course Title	**Circuits Simulation Lab**		
Course Code	**25BECAE307C**	**CIE Marks**	**50**
L: T: P	**0: 0: 30**	**SEE Marks**	**50**
Credits	**1**	**Exam Hours**	**3**

Course Learning Objectives: The purpose of the course is to facilitate the learner to:

- Understand the operation and characteristics of BJT and MOSFET devices.
- Analyze transistor amplifier circuits using appropriate small-signal models.
- Apply biasing techniques for stable operation of BJT and MOSFET amplifiers.
- Design and analyse linear and non-linear operational amplifier circuits for various applications.
- Study oscillator circuits and other applications for BJT, MOSEFETs and Op-amps

Sl. No	**Experiments**
1	Design a single-stage RC-coupled Common-Emitter (CE) amplifier using a silicon NPN transistor to achieve a specified midband voltage gain Assume the following specifications: Supply voltage: V_{CC}=10V Load resistance: RL=10 kΩ Transistor current gain: β=100 Lower cutoff frequency: fL≤100 Hz Midband voltage gain: |Av|≈ Show all design calculations, determine the transistor bias point, and verify the design using small-signal analysis.
2	Design a single-stage Common-Collector (Emitter Follower) amplifier using an NPN transistor to satisfy the following specifications: Supply voltage:VCC = 10V Transistor current gain: beta = 100 Load resistance: RL = 1k Quiescent emitter current: I_E = 2mA Lower cut-off frequency: 100Hz
3	Design an instrumentation amplifier.
4	Design a voltage regulator using operational amplifier to produce output of 12V with maximum load current of 50mA.
5	Design a Voltage to Current Converter using op-amp. Demonstrate floating load and ground load cases.

6	Design a precision amplifier using opamp.
7	Design an Inverting Schmitt Trigger. Calculate theoretical and practical (V_{UTP}) and (V_{LTP}).
8	Design and demonstrate Darlington emitter follower with/without bootstrapping.
9	Design an integrator and differentiator circuit using opamp
10	Design and set-up BJT/FET based Colpitts Oscillator.

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Apply the principles of BJT small-signal models to analyse the performance of single-stage transistor amplifiers and determine gain, input and output resistance.
CO2	Apply MOSFET device characteristics and biasing techniques to determine the operating point and analyse the behaviour of MOSFET amplifier circuits.
CO3	Apply operational amplifier principles to design and analyse linear circuits such as amplifiers, active filters, integrators, differentiators, and instrumentation amplifiers.
CO4	Analyze and implement some BJT and MOSFET based application circuits.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	20	-	Marks awarded for Weekly Conduction of Experiments and Submission of Laboratory records, scaled to 20 marks.
CIE Practical Test + Mini Project (B)	10 + 20	-	Test conducted for part A and part B, each carries 5 marks and final IA test conducted for 20 Marks
Total CIE (A+B)	**50**	**20**	**Sum of Marks of Experiments, Record and Test shall be CIE marks awarded for a maximum of 50.**
SEE (C)	**50**	**20**	**SEE is a lab exam conducted for 100 marks and scaled down to 50 marks. Exam duration shall be for 3 hours.**
CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

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B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – III			
Course Title	**Signals and Systems Lab**		
Course Code	**25BECAE307D**	**CIE Marks**	**50**
L: T: P	**0: 0: 30**	**SEE Marks**	**50**
Credits	**1**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Generate and perform basic operations on discrete-time signals effectively.
- Analyze linear time-invariant systems using convolution and its properties.
- Determine impulse, step, magnitude, and phase responses of systems.
- Apply Fourier transform techniques for discrete-time signal analysis.
- Evaluate signal characteristics using autocorrelation and cross-correlation techniques.

Sl. No	**Experiments**
1	Write a Matlab code to generate various standard signals.
2	Write a Matlab code to demonstrate various operation on Signals: Amplitude, scaling, Addition, Multiplication Time Shifting, Time Reflection.
3	Write a Matlab code of to demonstrate convolution of two given sequences without using inbuilt function.
4	Write a Matlab code: a. to perform verification of commutative property of convolution. b. to perform verification of distributive property of convolution. c. to perform verification of associative property of convolution.
5	Write a Matlab code to determine a) impulse b) Magnitude c) phase response from the difference equation representation of system.
6	Write a Matlab code to determine the step response from the impulse response of a system.
7	Write a Matlab code to generate square and triangular wave by summing fundamental and harmonics component.
8	Write a Matlab code to determine discrete time Fourier transform of a rectangular sequence.
9	Write a Matlab code to perform Auto correlation and verification of its properties.
10	Write a Matlab code to perform cross co- relation and verification of its properties.
11	Write a Matlab code to find Z-transform and inverse Z-transform of a sequence.
12	Write a Matlab code to solve difference equation of a system.

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Demonstrate the generation and graphical representation of discrete-time signals.
CO2	Apply signal processing operations and convolution techniques to analyze systems.
CO3	Evaluate the characteristics and responses of discrete-time systems.
CO4	Analyze signals and systems using Fourier and Z-transform methods.
CO5	Evaluate system behavior using correlation techniques and difference equations.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	20	-	Marks awarded for Weekly Conduction of Experiments and Submission of Laboratory records, scaled to 20 marks.
CIE Practical Test + Mini Project (B)	10 + 20	-	Test conducted for part A and part B, each carries 5 marks and final IA test conducted for 20 Marks
Total CIE (A+B)	**50**	**20**	**Sum of Marks of Experiments, Record and Test shall be CIE marks awarded for a maximum of 50.**
SEE (C)	**50**	**20**	**SEE is a lab exam conducted for 100 marks and scaled down to 50 marks. Exam duration shall be for 3 hours.**
CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – III			
Course Title	**NSS-National Service Scheme**		
Course Code	**25BNSSP309**	**CIE Marks**	**100**
SL	**30 Hrs/sem**	**SEE Marks**	**-**
Credits	**-**	**Exam Hours**	**-**
Course Learning Objectives: *The purpose of the course is to facilitate the learner to:* • Identify the needs and problems of the community and involve the problem–solving. • Develop among them a sense of social and civic responsibility and utilize their knowledge in finding practical solutions to individual and community problems. • Develop competence required for group-living and sharing of responsibilities and gain skills in mobilising community participation to acquire leadership qualities and democratic attitudes.			
Module 1			**6 hrs**
Introduction to NSS, Life Competencies, Youth Leadership and NSS			
Module 2			**6 hrs**
Social connect and responsibilities.			
Module 3			**6 hrs**
Activities -1 (Choose from Activity list)			
Module 4			**6 hrs**
Activities -2 (Choose from Activity list)			
Module 5			**6 hrs**
Activities -3 (Choose from Activity list)			

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Understand the motto and concepts of NSS
CO2	Develop overall personality of volunteers and make them as leaders and responsible citizens of our nation
CO3	Analyze the environmental and societal problems/issues and will be able to design solutions for the same.

CO4	Communicate effectively with the community and with the officials.

Activity list:

Sl. No	Activity	Deliverables
1	Plantation Drive: Adopt a Tree	Developing and managing an efficient garbage disposal system
2	Food Preservation/ Packaging awareness	Tourism Promotion: Innovative Approaches
3	Facilitating 100% digitized money transactions	Contribution to any national-level initiative of the Government of India. E.g. Digital India/ Skill India/ Swachh Bharat Internship etc.,

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	60	-	Sum of Two Internal Assessment Tests (MCQs) each conducted for 30 marks.
Continuous and Comprehensive Evaluation (B)	40	-	Any two assessment methods as per 24RNBE4.2, scaled to 40 marks.
CIE + SEE (A+B)	**100**	**40**	CIE Evaluation is done for a maximum of 100 marks
• The minimum marks to be secured in CIE is 40 (40%) out of 100 marks allotted to Pass.			

Text Books:

1.	NSS Course Manual, Published by NSS Cell, VTU Belagavi.
2.	Government of Karnataka, NSS cell, activities reports and its manual.
3.	Government of India, NSS cell, Activities reports and its manual.

Web links:

1.	https://nss.gov.in/
2.	https://pledge.mygov.in/

B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – III			
Course Title	**Physical Education**		
Course Code	**25BPEDU309**	**CIE Marks**	**100**
(L: T: P) + SL	**(0: 0: 0) + 30 Hrs / sem**	**SEE Marks**	**-**
Credits	**-**	**Exam Hours**	**-**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Understand the fundamental concepts of Physical Education, games and sports skills, Health, Nutrition and Fitness
- Familiarization of health-related Exercises, Sports for overall growth and development
- Participate in the competition at regional/state / national / international levels.
- Create consciousness among the students on Health, Fitness and Wellness in developing and maintaining a healthy lifestyle.

Module 1		**6 hrs**

Orientation

A. Meaning and Importance of Physical Education

B. Lifestyle

C. Health and Wellness

Module 2		**6 hrs**

General Fitness and Components of Fitness

A. Meaning and Importance of Fitness

B. Warming up (Free Hand exercises)

C. Strength – Push-up / Pull-ups

Module 3		**6 hrs**

Specific games (Anyone to be selected by the student)

A. Kabaddi

a) Fundamental skills

Hand touch, Toe Touch, Thigh Hold, Ankle hold and Bonus.

b) Offensive Skills:

Raiding, Hand Touch, Toe Touch, Dubki, Squat Thrust

c) Defensive Skills:

Tackling, Ankle Hold, Thigh Hold, Waist Hold, Blocking, Chain Tackle

d) Other Important Skills:

Agility, Speed, Breath Control, Breath Holding

e) Rules and their interpretation and duties of the officials

B. Kho-Kho

a) Fundamental skills

Giving Kho, Single Chain, Pole dive, Pole turning, 3-6 Up.

b) Skills in Chasing:

Sit on the box (Parallel & Bullet toe method), Get up from the box (Proximal & Distal foot method), Give Kho (Simple, Early, Late & Judgment), Pole Turn, Pole Dive, Tapping, Rectification of foul.

c) Skills in running:

Chain Play, Ring play and Chain & Ring mixed play.

d) Game practice with application of Rules and Regulations.

e) Rules and their interpretations and duties of the officials.

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Understand the fundamental concepts of Physical Education, games and sports skills, Health, Nutrition and Fitness
CO2	Familiarization of health-related Exercises, Sports for overall growth and development
CO3	Participate in the competition at regional/state/national/international levels.
CO4	Create consciousness among the students on Health, Fitness and Wellness in developing and maintaining a healthy lifestyle.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	60	-	Sum of Two Internal Assessment Tests (MCQs) each conducted for 30 marks.
Continuous and Comprehensive Evaluation (B)	40	-	Any two assessment methods as per 24RNBE4.2, scaled to 40 marks.
CIE + SEE (A+B)	**100**	**40**	CIE Evaluation is done for a maximum of 100 marks
• The minimum marks to be secured in CIE is 40 (40%) out of 100 marks allotted to Pass.			

Text Books:

1.	Saha, A. K. Sarir Siksher Ritiniti, Rana Publishing House, Kalyani.
2.	Bandopadhyay, K. Sarir Siksha Parichay, Classic Publishers, Kolkata.

Reference Books:

1.	Saraswati Health and Physical Education Textbook
2.	V.K. Sharma's Health and Physical Education

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B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – III			
Course Title	**Yoga**		
Course Code	**25BYOGA309**	**CIE Marks**	**100**
(L: T: P) + SL	**(0: 0: 0) + 30 Hrs / sem**	**SEE Marks**	**-**
Credits	**-**	**Exam Hours**	**-**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Physical, Mental & spiritual Objectives of Yoga
- Explain the meaning of Yoga.
- Discuss the importance of the Yoga and its scope.
- Describe the aims and objectives of Yoga.
- Clarify the misconceptions on Yoga

Module 1		**6 hrs**

Orientation

- Introduction of Yoga
- Aim, and Objectives of Yoga,
- Yoga, its origin, history and development.

Module 2		**6 hrs**

Yoga

- Yoga, its meaning, definitions.
- Brief introduction of yogic practices for the common man
- Rules and regulations
- Misconceptions of Yoga
- Suryanamaskara

Module 3		**6 hrs**

Asanas

Types of Asanas:

1.	**Sitting-**	1. Padmasana,	2. Vajrasana
2.	**Standing-**	1. Vrikshana,	2. Trikonasana
3.	**Prone line-**	1. Bhujangasana	2. Shalabh asana
4.	**Supine line-**	1. Utthita dvipadasana	2. Ardha halasana

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Understand the fundamental concepts of Yoga
CO2	Improves of health and related aspects, overall growth and development
CO3	Participate in the competition at regional/state/national/international levels.
CO4	Create consciousness among the students on Health, Fitness and Wellness in developing and maintaining a healthy lifestyle.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	60	-	Sum of Two Internal Assessment Tests (MCQs) each conducted for 30 marks.
Continuous and Comprehensive Evaluation (B)	40	-	Any two assessment methods as per 24RNBE4.2, scaled to 40 marks.
CIE + SEE (A+B)	**100**	**40**	CIE Evaluation is done for a maximum of 100 marks
• The minimum marks to be secured in CIE is 40 (40%) out of 100 marks allotted to Pass.			

Text Books:

1.	The Yoga Sutras of Patanjali – Sri Swami Satchidananda.
2.	Light on Yoga — B.K.S Iyengar.

Reference Books:

1.	The Heart of Yoga — T.K.V Desikachar.
2.	"Asana Pranayama Mudra Bandha" by Swami Satyananda Saraswati.

B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – III			
Course Title	**Music**		
Course Code	**25BMUSK309**	**CIE Marks**	**100**
(L: T: P) + SL	**(0: 0: 0) + 30 Hrs / sem**	**SEE Marks**	**-**
Credits	**-**	**Exam Hours**	**-**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Understand the origin, evolution, and fundamental concepts of Indian classical music.
- Familiarize themselves with the basic forms of Carnatic and Hindustani music compositions and appreciate their musical structure and significance.
- Identify and classify the major musical instruments used in Carnatic and Hindustani music and understand their construction and performance characteristics.
- Recognize the contributions of eminent Indian composers and musicians to the development and preservation of Indian classical music.
- Develop an appreciation for India's rich musical heritage, fostering creativity, cultural awareness, and lifelong interest in music.

Module 1		**6 hrs**
Origin of the Indian Music: Evolution of the Indian music system, Understanding of Shruthi, Nada, Swara, Laya, Raga Tala, Mela.		
Module 2		**6 hrs**
Compositions: Introduction to the few types of composition in Carnatic Music- Geethe, Swarajathi, Varna, Madhyama Kala Krithi,		
Module 3		**6 hrs**
Compositions: Introduction to the few types of composition in Hindustani Music: Khayal, Drupad, Tarana		
Module 4		**6 hrs**
Music Instruments: Classification and construction of string instruments, percussion instruments in both Carnatic and Hindustani Music.		
Module 5		**6 hrs**
Composers: Biography and contributions of the following eminent personalities Purandaradasa, Thyagaraja, Pt. Mallikarjun Mansur, Vidhushi Gangubhai Hangal		

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Explain the origin, evolution, and fundamental concepts of Indian classical music.
CO2	Compare and distinguish the characteristics of selected Carnatic and Hindustani music compositions.
CO3	Classify the major categories of Indian musical instruments and describe their construction and applications in Carnatic and Hindustani music.
CO4	Examine the contributions of eminent Composers/Musicians and appreciate their role in preserving and promoting Indian classical music.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	60	-	Sum of Two Internal Assessment Tests (MCQs) each conducted for 30 marks.
Continuous and Comprehensive Evaluation (B)	40	-	Any two assessment methods as per 24RNBE4.2, scaled to 40 marks.
CIE + SEE (A+B)	**100**	**40**	CIE Evaluation is done for a maximum of 100 marks
• The minimum marks to be secured in CIE is 40 (40%) out of 100 marks allotted to Pass.			

Text Books:

1.	Vidushi Vasantha Madhavi, "Theory of Music", Prism Publication, 2007.
2.	T Sachidevi and T Sharadha (Thirumalai Sisters), Karnataka Sangeetha Dharpana- Vol. 1 (English), Shreenivaas Prakaashana, 2018.
3.	B. Chaitanya Deva, An Introduction to Indian Music, Publications Division, Government of India, New Delhi.

Reference Books:

1.	Lakshminarayana Subramaniam, Viji Subramanaim, "Classical Music of India: A Practical Guige, Tranqueber 2018.
2.	R. Rangaramanuja Ayyangar, "History of South Indian (Carnatic) Music", Vipanci Charitable Trust; Third edition, 2019,

3.	Vamanrao H. Deshpande, Indian Musical Traditions: An Aesthetic Study of the Gharanas in Hindustani Music, Popular Prakashan, Mumbai.

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B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – III			
Course Title	**Mathematics course for Lateral Entry Students**		
Course Code	**25BMADP310**	**CIE Marks**	**100**
(L: T: P) + SL	**(14: 0: 0) + 14 Hours / Sem**	**SEE Marks**	**-**
Credits	**-**	**Exam Hours**	**-**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Apply the fundamental concepts of complex trigonometry, vector algebra, and differential and integral calculus to analyze mathematical and engineering problems.
- Apply the principles of vector differentiation and solve first-order ordinary differential equations in relevant scientific and engineering contexts.

Module 1	**Complex Trigonometry**	**3 hrs**
Complex Numbers: Definitions and properties. Modulus and amplitude of a complex number, Argand's diagram, De-Moivre's theorem (without proof). Vector Algebra: Scalar and vectors. Addition and subtraction and multiplication of vectors- Dot and Cross products, problems.		
Module 2	**Differential Calculus**	**3 hrs**
Review of successive differentiation-illustrative examples. Maclaurin's series expansions Illustrative examples. Partial Differentiation: Euler's theorem problems on first order derivatives only. Total derivatives-differentiation of composite functions. Jacobians of order two-Problems.		
Module 3	**Vector Differentiation**	**3 hrs**
Differentiation of vector functions. Velocity and acceleration of a particle moving on a space curve. Scalar and vector point functions. Gradient, Divergence, Curl-simple problems. Solenoidal and irrotational vector fields-Problems.		
Module 4	**Integral Calculus**	**3 hrs**
Review of elementary integral calculus. Reduction formulae for $\sin^n x$, $\cos^n x$ (with proof) and $\sin^m x \cos^n x$ (without proof) and evaluation of these with standard limits-Examples.		
Module 5	**Ordinary differential equations**	**2 hrs**
Introduction-solutions of first order and first-degree differential equations: exact, linear differential equations. Equations are reducible to exact and Bernoulli's equation.		

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Apply concepts of complex numbers and vector algebra to analyze the problems arising in related areas.
CO2	Apply derivatives and partial derivatives to calculate rate of change of multivariate functions.
CO3	Solve problems involving position, velocity, and acceleration in two- and three-dimensions using vector-valued functions.
CO4	Apply the fundamental techniques of elementary integration to solve standard integrals.
CO5	Identify and solve first order ordinary differential equations.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	60	-	Sum of Two Internal Assessment Tests (MCQs) each conducted for 30 marks.
Continuous and Comprehensive Evaluation (B)	40	-	Any two assessment methods as per 24RNBE4.2, scaled to 40 marks.
CIE + SEE (A+B)	**100**	**40**	CIE Evaluation is done for a maximum of 100 marks
• The minimum marks to be secured in CIE is 40 (40%) out of 100 marks allotted to Pass.			

Text Books:

1.	B. S. Grewal, "Higher Engineering Mathematics", Khanna Publishers, 43rd Edition, 2015.

Reference Books:

1.	E. Kreyszig, "Advanced Engineering Mathematics", John Wiley & Sons, 10th Edition, 2015
2.	N. P. Bali, Manish Goyal, "Engineering Mathematics", Laxmi Publishers, 7th Edition, 2007
3.	Rohit Khurana, "Engineering Mathematics", Vol. I, Cengage Learning, 1st Edition, 2015

Additional Mathematics I and II:

- These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semesters to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.
- Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.
- Successful completion of the courses Additional Mathematics I and II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics I and II shall be indicated as Unsatisfactory.

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B.E. (Electronics and Communication Engineering)

Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
Skill Development Course
SEMESTER-III

Course Title:	**VLSI and Embedded System**		
Course Code:	**25BECSL001**	**CIE MARKS**	**50**
L : T : P + (SL)	**0:0:30**	**SEE MARKS**	**50**
Credits:	**1**	**Exam Hours**	**3**

COURSE LEARNING OBJECTIVES: *The purpose of the course is to facilitate the learner to:*

- Explain the fundamentals of finite state machines and develop behavioural Verilog code to implement sequential digital systems using Vivado and Artix-7 FPGA.
- Design, simulate, and synthesize FSM-based applications using Verilog HDL.
- Design and study CMOS circuits, such as inverters, buffers, pass-transistor logic, and transmission gates, using Cadence tools.
- Analyse CMOS circuit performance by studying delay, power consumption, transistor sizing, voltage transfer characteristics, and MOSFET behaviour.
- Apply VLSI and digital design concepts to build practical projects involving FSMs, CMOS circuits, current mirrors, and current multipliers.

Sl no	Experiments / Hands-on learning
1.	Implementation of coffee vending machine/
2.	Implementation of coin phone booth
3.	Implementation of sequence detector.
4.	Implementation of Tea vending machine.
5.	Implementation of digital stop watch.
6.	Implementation of Pizza vending machine.
7.	Implementation of Pseudorandom sequence generator.
8.	Implementation of calculator.
9.	Implementation of Exam process.
10.	Implementation of Library book borrowing system.
11.	Implementation of Smart call handling system.
12.	Implementation of Online shopping system.
13.	Implementation of Airport Check in process.
14.	Implementation of Smart home thermostat.
15.	Implementation of ATM system.
16.	Implementation of Media player.
17.	Implementation of Login authentication flow.
18.	Implementation of Washing machine.
19.	Implementation of Rock, Paper, Scissor board game.
20.	Implementation of Chat bot conversation flow.
21.	Implementation of smart helmet for drowsiness detection, unauthorized access to vehicle
22.	Implementation of smart walking stick to guide a blind person
23.	Implementation of smart watch to monitor the vitals of patient.
24.	Implementation of smart cradle to monitor the babies sleep and prevent from falling.

25.	CMOS Inverter Design and Transistor Sizing Design a CMOS inverter and vary the PMOS-to-NMOS width ratio. • Plot the voltage transfer characteristic (VTC). • Measure switching threshold and noise margins. • Compare rise time, fall time and propagation delay. Deliverable: Graphs showing how transistor sizing affects inverter
26.	Design of a CMOS Buffer for a Large Capacitive Load Design a chain of inverters to drive a large load capacitance. • Compare a single inverter with a multistage buffer. • Vary the size ratio between successive stages. • Measure delay, power and area. Deliverable: The buffer sizing strategy that gives the best delay under an area or power constraint
27.	MOSFET I–V Characteristic Analyzer Simulate an NMOS and PMOS and study their drain-current characteristics. • Sweep VGS and plot ID versus VDS. • Repeat for different gate voltages. • Identify cut-off, linear and saturation regions. • Extract threshold voltage and trans-conductance. Outcome: MOSFET I–V curves and extracted device parameters.
28.	NMOS/PMOS Pass Transistor and the Weak Logic-1/Weak Logic-0 Problem Use a single NMOS transistor as a switch to transfer a digital input. • Apply logic 0 and logic 1 at the input. • Measure the output voltage. • Observe why a high output may be limited under simple operating assumptions. • Investigate the effect of body effect and supply voltage. Outcome: Demonstrate the voltage degradation associated with an NMOS pass transistor.
29.	Design and Analysis of a Pass-Transistor XOR Gate Implement an XOR gate using pass-transistor logic and compare it with a conventional CMOS implementation. • Verify the truth table. • Measure output-high and output-low levels. • 30Compare transistor count, propagation delay and power. • Check whether output restoration is required. Outcome: Understand the area and performance trade-offs of pass-transistor logic.
30.	Effect of Cascaded Pass Transistors on Logic Levels Connect multiple pass transistors in a chain and study signal degradation. • Measure output voltage after each stage. • Compare different transistor sizes. • Investigate the effect of load capacitance. • Propose a buffer or level-restoration solution. Outcome: Identify limitations when pass-transistor stages are cascaded.
31.	Design of a 2:1 Multiplexer Using Transmission Gates Implement a multiplexer using two transmission gates and an inverter for select control. • Verify all input/select combinations. • Measure propagation delay. • Compare transistor count and power with a conventional CMOS mux.

	• Investigate the effect of output load capacitance. Outcome: A functional transmission-gate multiplexer with performance measurements.
32.	Transmission-Gate Latch Build a level-sensitive latch using transmission gates and inverters. • Verify transparent and hold modes. • Study timing behaviour with a clock. • Measure propagation delay and setup/hold behaviour where applicable. • Examine how transistor sizing affects delay and power. Outcome: Understand how transmission gates are used in sequential CMOS circuits.
33.	Transmission-Gate D-Flipflop Build a Edge Sensitive-sensitive latch using transmission gates and inverters
34.	Design and Simulation of a CMOS Ring Oscillator
35.	Design and Characterization of a Basic CMOS Current Mirror Design a two-transistor NMOS current mirror and verify how accurately it copies a reference current. • Sweep the output voltage and plot output current. • Determine the minimum output voltage required for proper operation. • Measure current-mirror error and output resistance. • Study the effect of transistor sizing. Deliverable: Output-current-versus-output-voltage graph and current-mirror accuracy analysis.
36.	Design of a CMOS Current Multiplier Beginner Use transistor sizing ratios to generate an output current that is a multiple of the reference current. • Design ×1, ×2 and ×4 current outputs.
Demonstration Experiments (For CIE)	
1.	Introduction to State machines, Introduction to Behavioural style Verilog code.
2.	Implementation of traffic light system.
3.	Implementation of seat belt warning system
4.	Demonstration of drone Flight control system.
5.	Introduction to CMOS logic circuits, Transistor sizing in CMOS circuits, Effect of sizing on circuit performance, Hands on with small examples.
6.	Propagation delay in CMOS circuits, Factors affecting delay, Power calculation in CMOS circuits, hands on of Delay and power analysis.
7.	Characterization of MOSFET using parametric analysis, Pass transistors and Transmission Gate, DC characteristics of Ratioed and Ratioless logic circuit.
8.	Current mirrors and current multipliers(steering circuits)

COURSE OUTCOMES:

After successfully completing the course, the student will be able to:

CO1	Develop finite state machines using behavioural Verilog HDL for implementing sequential digital systems..
CO2	Simulate and synthesize FSM-based applications using Vivado and demonstrate their functionality on FPGA platforms.
CO3	Design and simulate CMOS logic circuits using Cadence tools, considering transistor sizing

	and circuit characteristics..
CO4	Analyse CMOS circuit performance in terms of propagation delay, power consumption, MOSFET characteristics, and logic-level behaviour.
CO5	Implement practical VLSI and digital system design projects using Verilog HDL and CMOS circuit design techniques.

Suggested Learning Resources:

1. Vivado Design Suite – User Guides and Tutorials.
For creating Verilog projects, running simulation, synthesis, implementation, and FPGA programming.
https://www.amd.com/en/developer/resources/vivado.html?utm_source=chatgpt.com

2. Embedded Design Tutorial (PDF/manual)
Official guide to embedded hardware design using Vivado and related tools.
https://docs.amd.com/r/2022.1-English/ug940-vivado-tutorial-embedded-design?utm_source=chatgpt.com

3. Cadence Academic Resources
Academic learning resources for circuit design, schematic entry, simulation, and IC design.

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B.E. (Electronics and Communication Engineering)
Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
Skill Development Course
SEMESTER-III

Course Title	**Signal Processing Applications with AI**		
Course Code	**25BECSL002**	**CIE Marks**	**50**
(L: T: P) + SL	**(0: 0: 30)**	**SEE Marks**	**50**
Credits	**1**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

Understand core signal-processing concepts and how MATLAB represents and analyse signals.
Use Signal Processing Toolbox functions to filter signals and design, analyse, and apply digital filters.
Perform frequency-domain analysis using Fourier transforms and spectral estimation.
Analyze signals in time and frequency domains using appropriate methods and visualizations.
Apply toolbox workflows to common tasks such as noise reduction, feature extraction, and signal measurement.

Module-1	**Signal Generation, Analysis, and Pre-processing**	**2 hrs**
Process a Signal with Missing Samples, Measure Signal Similarities, Align Signals with Different Start Times, Resample Uniformly and Non-uniformly Sampled Signals, Find a Signal in a Measurement.		
Module-2	**Waveform Generation, Signal Analysis and Visualization**	**2 hrs**
Compute Envelope Spectrum of Vibration Signal, **Experiment 1**: Extract Voices from Music Signal, **Experiment 2:** Extract Regions of Interest from Whale Song.		
Module-3	**Smoothing and Denoising**	**2 hrs**
Signal Smoothing, Remove Trends from Data, Remove the 60 Hz Hum from a Signal, Remove Spikes from a Signal, and Reconstruct a Signal from Irregularly Sampled Data.		
Module-4	**Measurements and Feature Extraction**	**2 hrs**
Distortion Measurements, Determine Peak Widths, **Experiment 3:** Classify ECG Signals Using Long Short-Term Memory Networks, **Experiment 4:** Human Activity Recognition Using Signal Feature Extraction and Machine Learning, **Experiment 5:** Waveform Segmentation Using Deep Learning.		
Module-5	**Descriptive Statistics**	**2 hrs**
Measure Signal Similarities, Extract Classification Features from Physiological Signals, Automate Signal Labelling with Custom Functions. **Capstone Project:** Human Activity Recognition Simulink Model for Smartphone Deployment.		
Module-6	**Transforms, Correlation, and Modelling**	
Single Sideband Modulation Using Hilbert Transform, DCT for Speech Signal Compression, Walsh-Hadamard Transform for Spectral Analysis and Compression of ECG Signals		

Module-7	**Time-Frequency Analysis**	
Waveform Segmentation Using Deep Learning, Spectral Descriptors. **Capstone Project** : Spoken Digit Recognition with Custom Log Spectrogram Layer and Deep Learning		
Module-8	**Vibration Analysis**	
Compute Envelope Spectrum of Vibration Signal, Vibration Analysis of Rotating Machinery. **Capstone Project:** Machine Learning and Deep Learning Classification Using Signal Feature Extraction Objects		
Module-9	**AI for Signals - I**	**2 Hrs**
CBRS Band Radar Detection in 5G Signals and Noise Using YOLOX. **Capstone Project** :Hand Gesture Classification Using Radar Signals and Deep Learning		
Module-10	**AI for Signals - II**	**2 Hrs**
Musical Instrument Classification with Joint Time-Frequency Scattering, Classify Arm Motions Using EMG Signals and Deep Learning, **Capstone Project** : Pedestrian and Bicyclist Classification Using Deep Learning		

COURSE OUTCOMES: After successfully completing the course, the student will be able to:	
CO1	Import, generate, and visualize signals in MATLAB using Signal Processing Toolbox functions.
CO2	Process noisy signals using appropriate filtering and noise-reduction techniques
CO3	Select suitable Signal Processing toolbox functions and AI workflows for signal-processing tasks.
CO4	Develop MATLAB scripts or live scripts to perform signal analysis and processing.
CO5	Evaluate and validate results using relevant plots, measurements, and performance criteria.

Suggested Learning Resources:

1. Signal Processing Toolbox Getting Started Guide
   (https://in.mathworks.com/help/releases/R2026b/pdf_doc/signal/signal_gs.pdf)
2. Signal Processing Toolbox User's Guide
   (https://in.mathworks.com/help/releases/R2026b/pdf_doc/signal/signal.pdf)
3. Signal Processing Toolbox Reference
   (https://in.mathworks.com/help/releases/R2026b/pdf_doc/signal/signal_ref.pdf)

IV SEMESTER COURSES

ESTD : 2001
An Institute with a Difference

B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – IV			
Course Title	**Mathematics for Machine Learning**		
Course Code	**25BECTH401**	**CIE Marks**	**50**
(L: T: P) + SL	**(45: 30: 0) + 45 Hours / Sem**	**SEE Marks**	**50**
Credits	**4**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Learn to use linear algebra, calculus, optimization which are having strong linkage with machine learning.
- Develop the knowledge of machine learning and their applications in decision making and analysis.
- Analyse and detect patterns in data which can then be utilized for predictions and for developing models.

Module-1	**Multivariate Calculus and Linear Regression**	**9 hrs**

Multivariate Calculus: Functions of several variables, gradients, Jacobian and Hessian matrices and Its Applications, Gradient descent and stochastic gradient descent.

Linear Regression: Parameter estimation, maximum likelihood estimation, overfitting in Linear Regression, Bayesian Linear Regression.

Module-2	**Linear Algebra I**	**9 hrs**

Introduction to Linear Algebra

Eigenvalues and Eigenvectors: Conceptual and geometric understanding of eigenvalues and eigenvectors; diagonalization and spectral decomposition; relevance in system stability, feature extraction.

Quadratic Forms and Matrix Properties: Definition and examples of quadratic forms; symmetric matrices and their spectral properties; conditions for positive definiteness and semi-definiteness. Applications.

Module-3	**Linear Algebra II**	**9 hrs**

Singular Value Decomposition (SVD): Mathematical formulation and interpretation, relation to eigen decomposition, applications in dimensionality reduction**.**

Principal Component Analysis (PCA): Concept and motivation for dimensionality reduction, connection with SVD and covariance matrix, use cases in data preprocessing and feature extraction.

Module-4	**Classical and Advanced Optimization**	**9 hrs**

Constrained and Unconstrained Optimization: Lagrange's method of Multipliers, Method of steepest ascent/descent, Newton's method.

Momentum-based gradient descent methods: Adagrad, RMSprop and Adam, Understanding Moving Average, Exponential Moving Average.		
Module-5	**Descriptive and Inferential Statistics**	**9 hrs**
Descriptive Statistics: Measures of central tendency: mean, median, mode – A revision **Inferential Statistics:** Sampling and sampling distributions, confidence intervals, hypothesis testing (null and alternate), t-tests, z-tests and Chi-square test.		

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Apply multivariate calculus techniques and implement linear regression models, including regularization and optimization methods.
CO2	Understand and apply concepts of matrices and quadratic forms and eigen values to analyse data structures and transformations in machine learning. extract features, and improve the performance and interpretability of machine learning models.
CO3	Apply Singular Value Decomposition (SVD) and Principal Component Analysis (PCA) to reduce dimensionality, extract features, and improve the performance and interpretability of machine learning models.
CO4	Apply suitable optimization techniques for machine learning and deep learning models based on problem characteristics.
CO5	Understand and interpret data using descriptive and inferential statistics to support evidence-based decision making.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	30	-	Two tests each of 50 marks shall be conducted. Average of Two Internal Assessment Tests shall be scaled down to 30 marks.
Continuous and Comprehensive Evaluation (B)	20	-	Any two Assessment methods as per 24RNBE4.2 (*if it is project based, one assignment shall be given), scaled to 20 marks.
Total CIE (A+B)	**50**	**20**	**CIE Evaluation is done for a maximum of 50 marks**
SEE (C)	**50**	**18**	**SEE is a theory exam conducted for 100 marks and scaled down to 50**

			marks. Exam duration shall be for 3 hours.
CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

Text Books:

1.	Marc Peter Deisenroth, A. Aldo Faisal, and Cheng Soon Ong, "Mathematics for Machine Learning", Cambridge University Press, 2020.
2.	B. S. Grewal, "Higher Engineering Mathematics", Khanna Publishers, 44th Ed., 2021.
3.	Gilbert Strang, "Linear Algebra and Learning from Data", Wellesley-Cambridge Press, 2019.
4.	Ian Goodfellow, Yoshua Bengio, and Courville "Deep Learning", The MIT Press, 1st Edition, 2016

Reference Books:

1.	David C. Lay, "Linear Algebra and Its Applications", Pearson, 5th Edition.
2.	Kevin P. Murphy, "Machine Learning: A Probabilistic Perspective", MIT Press, 2012.
3.	Gareth James, Daniela Witten, Trevor Hastie and Robert Tibshirani, "An Introduction to Statistical Learning", Springer, Second Edition.
4.	Sheldon M. Ross, "Introduction to Probability and Statistics for Engineers and Scientists", Academic Press (2020) 6th edition.

Weblinks and Video Lectures:

1.	https://onlinecourses.nptel.ac.in/e-learning/preview/noc26_ma97
2.	https://onlinecourses.nptel.ac.in/e-learning/preview/noc26_ma129
3.	https://www.youtube.com/results?search_query=gilbert+strang

B.E. (Electronics and Communication Engineering)
Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
SEMESTER – IV

Course Title	**Digital Signal Processing**		
Course Code	**25BECIC402**	**CIE Marks**	**50**
(L: T: P) + SL	**(45: 0: 30) + 45 Hours / Sem**	**SEE Marks**	**50**
Credits	**4**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Understand frequency-domain analysis of discrete-time signals using the Discrete Fourier Transform (DFT) and its fundamental properties for signal representation and reconstruction.
- Apply efficient computational techniques such as Fast Fourier Transform (FFT) algorithms for analyzing and processing discrete-time signals.
- Design and analyze FIR (Finite Impulse Response) filters using windowing techniques and understand their structures for practical signal processing applications.
- Develop IIR (Infinite Impulse Response) filters using methods like Bilinear Transformation and analog-to-digital filter conversion techniques.
- Explore multirate signal processing concepts and real-world DSP applications, particularly in areas such as biomedical signal processing and voice processing.

Module-1	**Discrete Fourier Transforms**	**9 hrs**

Frequency domain sampling and Reconstruction of Discrete Time Signals, The Discrete Fourier Transform, DFT as a linear transformation, Properties of the DFT: Periodicity, Linearity and Symmetry properties, Multiplication of two DFTs and Circular Convolution.

Text 1

Module-2	**Additional DFT Properties, Linear filtering, and FFT**	**9 hrs**

Additional DFT Properties, Linear filtering methods based on the DFT: Use of DFT in Linear Filtering, Filtering of Long data Sequences. Fast-Fourier-Transform (FFT) algorithms: Efficient Computation of the DFT: Radix-2 FFT algorithms for the computation of DFT and IDFT decimation intime.

Text 1

Module-3	**Design of FIR Filters**	**9 hrs**

Characteristics of practical frequency-selective filters, Symmetric and Antisymmetric FIR filters, Design of Linear-phase FIR (low pass and High pass) filters using windows - Rectangular, Hamming, Hanning, Bartlett windows. Structure for FIR Systems: Direct form, Cascade form and Lattice structures.

Text 1

Module-4	**IIR Filter Design**	**9 hrs**
Infinite Impulse response Filter Format, Bilinear Transformation Design Method, Analog Filters using Low pass prototype transformation, Normalized Butterworth Functions, Bilinear Transformation and Frequency Warping, Bilinear Transformation Design Procedure, Digital Butterworth (Lowpass and Highpass) Filter Design using BLT. Realization of IIR Filters in Direct form I and II **Text 1**		
Module-5	**Multirate Digital Signal Processing and Applications**	**9 hrs**
Introduction, Sampling, Sampling rate conversion, Signal flow graphs, Applications of DSP in biomedical Engineering, voice processing. **Text 2**		

PRACTICAL COMPONENT OF IPCC:

(List of Programs to be implemented & executed using any programming languages like C++/Python/Java/Scilab / MATLAB/CC Studio (but not limited to))

Sl. No	**Programs**
1	Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum.
2	Computation of circular convolution of two given sequences using DFT and IDFT.
3	Verification of Linearity property, circular time shift property & circular frequency shift property of DFT.
4	Verification of Parseval's theorem.
5	Design and implementation of IIR (Butterworth) low pass filter to meet given specifications.
6	Design and implementation of IIR (Butterworth) high pass filter to meet given specifications.
7	Design and implementation of low pass FIR filter to meet given specifications.
8	Design and implementation of high pass FIR filter to meet given specifications.
9	Design and implementation of BPF/BRF FIR filter to meet given specifications.
10	Implementation of decimation- interpolation operation on DTS.

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Determine response of LTI systems using time domain and DFT techniques

CO2	Compute DFT of real and complex discrete time signals
CO3	Compute DFT using FFT algorithms
CO4	Design FIR and IIR Digital Filters
CO5	Design and evaluate DSP solutions for biomedical and voice processing applications

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE- IA Tests (A)	20	-	Two tests each of 50 marks shall be conducted. Average of Two Internal Assessment Tests shall be scaled down to 20 marks.
Continuous and Comprehensive Evaluation (B)	10	-	Any one Assessment method as per 24RNBE4.2 scaled to 10 marks.
Total CIE Theory (A+B)	**30**	**12**	**Marks of Tests and Assignments awarded for a maximum of 30.**
CIE Practical	12	-	Marks awarded for Weekly Conduction of Experiments and Submission of Laboratory records, scaled to 12 marks.
CIE Practical Test	8	-	Average of marks of Two tests, each conducted for 100 marks covering all experiments, scaled to 8.
Total CIE Practical (C)	**20**	**8**	**Marks of Experiments, Record and Test awarded for a maximum of 20 marks.**
CIE: Theory + Practical (A+B+C)	**50**	**20**	**CIE Evaluation is done for a maximum of 50 marks.**
SEE (D)	**50**	**18**	**SEE is a theory exam, conducted for 100 marks and scaled down to 50 marks. Exam duration shall before 3 hours.**

CIE+SEE (A+B+C+D)	**100**	**40**	**Final marks shall be the sum of marks scored in Components A, B, C and D**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE. The laboratory component of the IPCC shall be for CIE only. However, in SEE, the questions from the laboratory component shall be included in their respective modules only.			

Text Books:

1.	Proakis & Manolakis, "Digital Signal Processing - Principles Algorithms & Applications", 4th Edition, Pearson education, New Delhi, 2007. ISBN: 81-317-1000-9
2.	Shalivahanan S, Gnanapriya C, "Digital Signal Processing", 2nd Edition, 2000, Tata McGraw-Hill Publication.

Reference Books:

1.	Sanjit K Mitra, "Digital Signal Processing, A Computer Based Approach", 4th Edition. McGraw Hill Education, 2013
2.	Oppenheim & Schaffer, "Discrete Time Signal Processing", PHI, 2003
3.	Li Tan, Jean Jiang, "Digital Signal processing - Fundamentals and Applications", Academic Press, 2013, ISBN: 978-0-12-415893.
4.	D Ganesh Rao and Vineeth P Gejji, "Digital Signal Processing" Cengage India Private Limited, 2017, ISBN: 9386858231.

Weblinks and Video Lectures:

1.	https://onlinecourses.nptel.ac.in/noc21_ee20/preview
2.	https://onlinecourses.nptel.ac.in/noc26_ee50/preview

B.E. (Electronics and Communication Engineering)
Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
SEMESTER – IV

Course Title	**Communication Systems**		
Course Code	**25BECTH403**	**CIE Marks**	**50**
(L: T: P) + SL	**(45: 30: 0) + (45 Hours / Sem)**	**SEE Marks**	**50**
Credits	**4**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Understand and analyse the principles and performance of analog modulation and demodulation techniques such as AM and FM used in communication systems.
- Analyse and evaluate digital signal formatting processes including sampling, quantization, pulse modulation techniques, and the effects of quantization noise.
- Evaluate the impact of channel noise on communication systems and analyse signal detection, recovery, and reconstruction techniques under noisy channel conditions.
- Apply and analyse the fundamental concepts of Information Theory, including entropy, source coding theorem, mutual information, channel capacity, and source coding techniques for efficient information representation.
- Analyse and design channel coding techniques, including linear block codes, cyclic codes, and convolutional codes, for error detection, error correction, and reliable digital communication.

Prerequisites: *Signals and Systems, Fourier Series, Fourier Transform.*

Module-1	**Amplitude Modulation**	**9 hrs**

Amplitude Modulation: Introduction, Amplitude Modulation: Time & Frequency Domain description, switching modulator, Envelope detector.

Double Sideband-Suppressed Carrier Modulation: Time and Frequency Domain description, Ring modulator, Coherent detection, Costas Receiver, Quadrature Carrier Multiplexing.

Single Side–Band and Vestigial Sideband Methods of Modulation (Qualitative).

Self-Study: Application of VSB, Frequency Translation, Frequency Division Multiplexing.

Module-2	**Angle Modulation**	**9 hrs**

Angle Modulation: Basic definitions, Frequency Modulation: Narrow Band FM, Wide Band FM, Transmission bandwidth of FM Signals, Generation of FM Signals, Demodulation of FM Signals.

Phase–Locked Loop: Nonlinear model of PLL, Linear model of PLL, Nonlinear Effects in FM Systems.

Self-Study: The Superheterodyne Receiver, Analog and Digital FM, Cellular Telephones

Module-3	**Sampling and Quantization**	**9 hrs**

Sampling and Quantization: Introduction, why digitize Analog sources? The Low pass sampling process (Qualitative and waveform approach), Pulse Amplitude modulation, Time Division Multiplexing, Pulse position Modulation, Generation of PPM waves, Detection of PPM waves, The Quantization Process, Pulse Code Modulation.		
Module-4	**Information Theory and Source Coding**	**9 hrs**
Introduction, Entropy, Source Coding Theorem, Lossless Data Compression Algorithms, Discrete Memoryless Channels, Mutual Information, Channel capacity, Channel Coding Theorem, Information Capacity Law (Statement).		
Module-5	**Channel Encoding**	**9 hrs**
Error Control Coding: Error Control Using Forward Error Correction. **Linear Block Codes:** Definitions, Matrix Descriptions, Syndrome and its properties, Minimum distance Considerations, Syndrome Decoding, Hamming Codes. *Self-Study: Cyclic Codes*		

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Analyse and evaluate the performance of Analog modulation and demodulation techniques such as AM and FM.
CO2	Analyse digital formatting processes including sampling, quantization, encoding, and quantization noise effects.
CO3	Evaluate the impact of channel noise on communication systems and analyse signal detection and reconstruction techniques.
CO4	Apply Information Theory concepts including entropy, source coding theorem, mutual information, and channel capacity in communication system analysis.
CO5	Analyse and design source coding and channel coding techniques, including linear block codes, cyclic codes, and convolutional codes, for efficient and reliable data transmission.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	30	-	Two tests each of 50 marks shall be conducted. Average of Two Internal Assessment Tests shall be scaled down to 30 marks.

Continuous and Comprehensive Evaluation (B)	20	-	Any two Assessment methods as per 24RNBE4.2 (*if it is project based, one assignment shall be given), scaled to 20 marks.
Total CIE (A+B)	**50**	**20**	**CIE Evaluation is done for a maximum of 50 marks**
SEE (C)	**50**	**18**	**SEE is a theory exam conducted for 100 marks and scaled down to 50 marks. Exam duration shall be for 3 hours.**
CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

Text Books:

1.	Simon Haykin, Communication Systems, 5th Edition, Wiley India, 2010.

Reference Books:

1.	B.P. Lathi and Zhi Ding, Modern Digital and Analog Communication Systems, 4th Edition, Oxford University Press, 2009.
2.	K. Sam Shanmugam, Digital and Analog Communication Systems, 1st Edition, Wiley India Pvt. Ltd., New Delhi, 2005.
3.	John G. Proakis and Masoud Salehi, Digital Communications, 5th Edition, McGraw-Hill Education, 2008.

Weblinks and Video Lectures:

1.	Principles of Communication Systems Part II, https://onlinecourses.nptel.ac.in/noc19_ee47/preview

B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – IV			
Course Title	**Control Systems**		
Course Code	**25BECTH404**	**CIE Marks**	**50**
(L: T: P) + SL	**(45: 30: 0) + 45 Hours / Sem**	**SEE Marks**	**50**
Credits	**4**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Represent the control systems using differential equations, transfer functions, block diagrams and signal flow graphs.
- Analyze the first and second order systems through their step responses.
- Apply various techniques such as Routh's criterion, Root locus, Bode plots to determine the stability of systems and the range of system parameter for systems to be stable.
- Represent the systems using state variables and solve the state equations.

Prerequisite/s: Laplace Transform and its applications

Module-1	**Mathematical Modeling of Physical Systems**	**9 hrs**

Definition of control system, open-loop and closed-loop control systems, automatic control systems, examples, mathematical modelling of physical systems, differential equation representation of translational and rotational systems, analogous electrical systems

Module-2	**Block Diagram and Signal Flow Graph representations of systems**	**9 hrs**

Determination of transfer functions of mechanical and analogous electrical systems, representation of systems using block diagrams, reduction of block diagram and determination of transfer functions, signal flow graphs, determination of transmission gain using Mason's gain formula

Module-3	**Time Response Analysis**	**9 hrs**

Standard test signals, first order system, example, step response of first order system, second order system, example, step response of second order system (underdamped, undamped, critically damped and overdamped), time response specifications: delay time, rise time, peak time, peak overshoot, settling time, steady state error and error coefficients, qualitative discussion on P, PI, PD and PID controllers

Module-4	**Stability Analysis**	**9 hrs**

Routh's criterion: Definitions of absolutely stable, marginally or critically stable, unstable system, relative stability, impulse response variation and location of poles for the kinds of systems mentioned, Routh's stability criterion, examples of leading element of a row going to zero in the Routh's array, all elements of a row going to zero, determination of frequency of oscillations, range

of system gain K for a system to be stable, for zero, one or two roots of characteristic equation on the RHS of s-plane, relative stability analysis **Root locus techniques:** Root locus construction rules, examples of systems wherein corresponding root loci may lie on real axis, have angles of departure, have angles of arrival, cross imaginary axis, examples of determining the range of system gain K for the system to be stable, to be damped oscillatory, etc.		
Module-5	**Frequency Response Analysis and State-Space Analysis**	**9 hrs**
Correlation between time and frequency response parameters: Frequency response of a second order system, derivation of $u_r(\omega_r)$, M_r , $u_b(\omega_b)$, relationship between time-response and frequency response parameters through damping factor **Bode Plots:** Construction of Bode magnitude and phase plots for the loop transfer function of a closed loop system, gain and phase crossover frequencies, gain and phase margins, determination of stability of a system, determination of system gain K for a given gain margin, phase margin and gain crossover frequency **State-Space analysis:** Drawbacks of transfer function representation of systems, concept of state, state-variables and state equation, determination of state model of the systems represented by differential equations, transfer functions, signal flow graphs, RLC circuits, mechanical systems, state transition matrix and its properties, solution of state equations using time-domain and transform-domain approaches		

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Apply fundamental principles to represent mechanical and electrical systems using differential equations.
CO2	Apply block diagram reduction techniques and Mason's gain formula to determine transfer function of systems.
CO3	Analyze the first and second order systems in time-domain, determine steady state error and error constants.
CO4	Analyze a given system using Routh's criterion or Root locus techniques to determine stability and system gain K for a specific requirement.
CO5	Perform frequency response analysis to determine a system's stability aspects, apply the concept of state and state-variables to obtain state-model of a system and solve state equations.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details

CIE – IA Tests (A)	30	-	Two tests each of 50 marks shall be conducted. Average of Two Internal Assessment Tests shall be scaled down to 30 marks.
Continuous and Comprehensive Evaluation (B)	20	-	Any two Assessment methods as per 24RNBE4.2 (*if it is project based, one assignment shall be given), scaled to 20 marks.
Total CIE (A+B)	**50**	**20**	**CIE Evaluation is done for a maximum of 50 marks**
SEE (C)	**50**	**18**	**SEE is a theory exam conducted for 100 marks and scaled down to 50 marks. Exam duration shall be for 3 hours.**
CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

Text Books:

1.	I. J. Nagrath and M Gopal, "Control Systems Engineering", New Age International Publishers, 8th edition, 2024.

Reference Books:

1.	A Nagoor Kani, "Control Systems Engineering", CBS publishers and distributors, 2nd edition, 2020.
2.	K Ogata, "Modern Control Engineering", Pearson Education India, 5th edition, 2015.
3.	Joseph Distefano III, Allen Stubberud and Evan Williams, "Control Systems (Schaum's Outline Series)", Mc Graw Hill Education, 3rd edition, 2003.

Weblinks and Video Lectures:

1.	https://nptel.ac.in/courses/107106081

B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – IV			
Course Title	**Communication Lab**		
Course Code	**25BECLB405**	**CIE Marks**	**50**
L: T: P	**0: 0: 30**	**SEE Marks**	**50**
Credits	**1**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the laboratory is to enable students to:

- Understand the generation and detection of analog modulation schemes such as AM and FM using simulation and hardware tools.
- Analyze the characteristics and performance of pulse modulation techniques, sampling, and quantization processes.
- Evaluate the effects of noise on communication systems and investigate signal recovery techniques.
- Implement and analyse information-theoretic concepts and source coding techniques for efficient data representation.
- Design and evaluate channel coding techniques for error detection and correction in digital communication systems.

Sl. No	**Experiments**
1	Basic Signals and Signal Graphing a) Unit Step b) Rectangular c) Standard Triangle d) Sinusoidal e) Exponential Signal
2	Illustration of signal representation in time and frequency domains for a rectangular pulse.
3	Amplitude Modulation and Demodulation: Generation and display the relevant signals and its spectrum.
4	Frequency Modulation and Demodulation: Generation and display the relevant signals and its spectrum.
5	Sampling and reconstruction of low pass signals. Display the signals and its spectrum.
6	PCM illustration: Sampling, Quantization and Encoding.
7	Encoding and Decoding of Huffman code.
8	Encoding and Decoding of binary data using a Hamming code.
9	Implementation and analysis of Cyclic Codes using CRC-CCITT generator polynomial. Perform encoding, syndrome computation, and error detection for error-free and erroneous received codewords.
10	Encoding and Decoding of Convolution code

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Implement and analyse AM and FM modulation and demodulation systems and evaluate their performance characteristics.
CO2	Perform sampling, quantization, PAM, PPM, and PCM operations and analyse the effects of digitization on signal quality.
CO3	Analyse the impact of noise on communication signals and evaluate signal detection and reconstruction techniques.
CO4	Apply information theory and source coding concepts to determine entropy, coding efficiency, and data compression performance.
CO5	Design and implement channel coding schemes such as linear block codes, cyclic codes, and convolutional codes for error detection and correction.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	20	-	Marks awarded for Weekly Conduction of Experiments and Submission of Laboratory records, scaled to 20 marks.
CIE Practical Test + Mini Project (B)	10 + 20	-	Test conducted for part A and part B, each carries 5 marks and final IA test conducted for 20 Marks
Total CIE (A+B)	**50**	**20**	**Sum of Marks of Experiments, Record and Test shall be CIE marks awarded for a maximum of 50.**
SEE (C)	**50**	**20**	**SEE is a lab exam conducted for 100 marks and scaled down to 50 marks. Exam duration shall be for 3 hours.**
CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

Text Books:

1.	Simon Haykin, Communication Systems, 5th Edition, Wiley India, 2010.
2.	K. Sam Shanmugam, Digital and Analog Communication Systems, 1st Edition, Wiley India Pvt. Ltd., New Delhi, 2005.

3.	John G. Proakis and Masoud Salehi, Digital Communications, 5th Edition, McGraw-Hill Education, 2008.

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B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – IV			
Course Title	**Machine Learning Lab**		
Course Code	**25BECAE406A**	**CIE Marks**	**50**
L: T: P	**0: 0: 30**	**SEE Marks**	**50**
Credits	**1**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Perform data preprocessing, feature engineering, and exploratory analysis to prepare real-world datasets for machine learning applications.
- Implement and evaluate supervised learning algorithms for regression and classification tasks using appropriate performance metrics.
- Apply concept learning, decision tree induction, and knowledge representation techniques to solve intelligent system problems.
- Analyze the behavior and performance of machine learning models by investigating issues such as overfitting, underfitting, model complexity, and error patterns.
- Develop end-to-end machine learning solutions by integrating data preparation, model training, validation, optimization, and result interpretation on real-world datasets.

Sl. No	Experiments
1	To perform data preprocessing and feature engineering on a real-world dataset by handling missing values, encoding categorical variables, and scaling features for machine learning.
2	To examine different types of machine learning approaches (Supervised, Unsupervised, Semi-supervised, and Reinforcement Learning) by setting up a basic classification problem and exploring how each type applies differently.
3	To implement and compare Linear Regression and Logistic Regression models on suitable datasets, and evaluate their performance using appropriate evaluation metrics.
4	To apply the Find-S and Candidate Elimination algorithms to a concept learning task and compare their inductive biases and outputs.
5	To construct a decision tree using the ID3 algorithm on a simple classification dataset.
6	To assess how the ID3 algorithm performs on datasets with varying characteristics and complexity, examining overfitting, underfitting, and decision tree depth.
7	To implement and compare Linear Regression and Polynomial Regression models on a real-world dataset, and evaluate them using appropriate regression metrics.
8	To represent and evaluate different scenarios using predicate logic and knowledge rules.

9	To go through all stages of a real-life machine learning project, from data collection to model fine-tuning, using a regression dataset like the California Housing Prices.
10	To perform binary and multiclass classification on the MNIST dataset, analyze performance metrics, and perform error analysis.

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Apply data preprocessing and feature engineering techniques to prepare datasets for machine learning applications.
CO2	Implement and evaluate machine learning algorithms for regression, classification, and concept learning tasks.
CO3	Analyze and compare different machine learning approaches and models using appropriate evaluation metrics.
CO4	Apply decision tree induction and knowledge representation techniques for intelligent decision-making systems.
CO5	Develop complete machine learning workflows for solving real-world problems through model building, optimization, and performance analysis.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – Practical (A)	30	-	Marks awarded for Weekly Conduction of Experiments and Submission of Laboratory records, scaled to 20 marks.
CIE Practical Test (B)	20	-	Test conducted for part A and part B, each carries 5 marks and final IA test conducted for 20 Marks
Total CIE (A+B)	**50**	**20**	**Sum of Marks of Experiments, Record and Test shall be CIE marks awarded for a maximum of 50.**
SEE (C)	**50**	**20**	**SEE is a lab exam conducted for 100 marks and scaled down to 50 marks. Exam duration shall be for 3 hours.**
CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

Text Books:

1.	Tom M. Mitchell, Machine Learning, First Edition, McGraw-Hill Education (India Edition), 1997.
2.	Aurélien Géron, Hands-On Machine Learning with Scikit-Learn, Keras, and TensorFlow, 3rd Edition, O'Reilly Media, 2022.

ESTD : 2001
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B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – IV			
Course Title	**Control Systems Lab**		
Course Code	**25BECAE406B**	**CIE Marks**	**50**
L: T: P	**0: 0: 30**	**SEE Marks**	**50**
Credits	**1**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Use the Software tool for learning the concepts of Control systems.
- Implement the models of Control systems
- Analyze the systems using various techniques

Sl. No	**Experiments (MATLAB / MATLAB SIMULINK or equivalent tool to be used)**
1	Implement the block diagram representation of a system and determine the transfer function.
2	Implement the given signal flow graph of a system and determine the transmission gain.
3	Obtain the time-response of a second order system and determine the time-response specifications
4	Implement the P, PI, PD and PID controllers, obtain their time-responses and comment on the rise-times, overshoots and settling times.
5	Obtain the frequency-response of a second order system and determine the frequency-response parameters
6	Determine the stability of given system using Routh's criterion.
7	Determination of stability of given system and the value / range of system gain K for a specific requirement (for system to be stable, damped oscillations, on imaginary axis, etc) using Root locus techniques
8	Determine the Gain margin, Phase margin and hence stability of a closed loop system represented by its loop transfer function using Bode plots
9	Solve the given state equation of a SISO system.
10	Design and implement a lead compensator and obtain its frequency response
11	Design and implement a lag compensator and obtain its frequency response
12	Design and implement a lag-lead compensator and obtain its frequency response

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Realize Control system concepts using the Software tool
CO2	Implement models of Control systems using the Software tool
CO3	Analyse the Control systems through various techniques.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – Record (A)	30	-	Marks awarded for Weekly Conduction of Experiments and Submission of Laboratory records, scaled to 30 marks.
CIE Practical Test (B)	20	-	Average of marks of Two tests, each conducted for 100 marks covering all experiments, scaled to 20.
Total CIE (A+B)	**50**	**20**	**Sum of Marks of Experiments, Record and Test shall be CIE marks awarded for a maximum of 50.**
SEE (C)	**50**	**20**	**SEE is a lab exam conducted for 100 marks and scaled down to 50 marks. Exam duration shall be for 3 hours.**
CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

Text Books:

1.	I. J. Nagrath and M Gopal, "Control Systems Engineering", New Age International Publishers, 8th edition, 2024.

Reference Books:

1.	A Nagoor Kani, "Control Systems Engineering", CBS publishers and distributors, 2nd edition, 2020.
2.	K Ogata, "Modern Control Engineering", Pearson Education India, 5th edition, 2015.
3.	Joseph Distefano III, Allen Stubberud and Evan Williams, "Control Systems (Schaum's Outline Series)", Mc Graw Hill Education, 3rd edition, 2003.

Weblinks and Video Lectures:

1.	https://nptel.ac.in/courses/107106081

ESTD : 2001
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B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – IV			
Course Title	**FPGA Based Systems Lab**		
Course Code	**25BECAE406C**	**CIE Marks**	**50**
L: T: P	**0: 0: 30**	**SEE Marks**	**50**
Credits	**1**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- To provide practical exposure to the students on executing and debugging various combinational and sequential circuits.
- To give the knowledge and practical exposure on applications of Digital Electronics.
- Program FPGAs/CPLDs to synthesize the digital circuits.
- Interface hardware to programmable ICS through I/O ports.

Sl. No	**Experiments**
1	Write a Verilog description to initialize even memory locations with 0 and odd memory locations with 1 using a for loop.
2	Write a Verilog description to count from 0 to 127 using a while loop and also display the count.
3	Write Verilog code to compute the factorial of a 4-bit number using task and function.
4	Write Verilog code to calculate the parity of a 32-bit register using function.
5	Write Verilog code to illustrate the execution of sequential blocks with and without delay sequential and parallel blocks.
6	Simulate and synthesize a Verilog program to generate pseudorandom sequence generators.
7	Simulate and synthesize a Verilog program for Ring and Johnson counters.
8	Write a Verilog program to design a Clock division circuit to perform 1⁄2, 1/3rd and 1⁄4th clock division of the given input clock. Verify on CRO by synthesizing the code.
9	Simulate and synthesize a Verilog program to implement Carry Lookahead Adder for 4-bit numbers.
10	Simulate and synthesize a Verilog program to implement Booth's algorithm for 4-bit numbers.
11	Verilog Program to interface DAC to FPGA to generate Square, Triangular and Sine waveforms.
12	Verilog Program to interface Seven segment Display to FPGA to display 0 to F.
13	Verilog Program to interface to FPGA to implement Elevator Control.
14	Verilog Program to interface 4 X4 keyboard FPGA to identify key pressed.

15	Verilog Program to interface a DC motor to FPGA and vary the speed of the motor.

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Design, simulate and synthesize combinational circuits. Verify the code using Test Bench and FPGA.
CO2	Design, simulate and synthesize Sequential circuits. Verify the code using Test Bench and FPGA.
CO3	Design and simulate delays, Functions and tasks in Verilog. Verify the code using Test Bench and FPGA.
CO4	Design and synthesize HDL program to interface various hardware circuits.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – Record (A)	30	-	Marks awarded for Weekly Conduction of Experiments and Submission of Laboratory records, scaled to 30 marks.
CIE Practical Test (B)	20	-	Average of marks of Two tests, each conducted for 100 marks covering all experiments, scaled to 20.
Total CIE (A+B)	**50**	**20**	**Sum of Marks of Experiments, Record and Test shall be CIE marks awarded for a maximum of 50.**
SEE (C)	**50**	**20**	**SEE is a lab exam conducted for 100 marks and scaled down to 50 marks. Exam duration shall be for 3 hours.**
CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

Text Books:

1.	Samir Palnitkar, "Verilog HDL: A Guide to Digital Design and Synthesis", Pearson Education, Second Edition.
2.	Nazeih M Botros, "HDL Programming VHDL and Verilog" Edition 2009, Dreamtech Press.

Reference Books:

1.	Donald E. Thomas, Philip R. Moorby, "The Verilog Hardware Description Language", Springer Science Business Media, LLC, Fifth edition.
2.	Michael D. Ciletti, "Advanced Digital Design with the Verilog HDL" Pearson (Prentice Hall), Second edition.
3.	Padmanabhan, Tripura Sundari, "Design through Verilog HDL", Wiley, 2016.

Weblinks and Video Lectures:

1.	https://onlinecourses.nptel.ac.in/e-learning/preview/noc24_cs61

ESTD : 2001
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B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – IV			
Course Title	**Graphical Programming Using LabVIEW**		
Course Code	**25BECAE406D**	**CIE Marks**	**50**
L: T: P	**0: 0: 30**	**SEE Marks**	**50**
Credits	**1**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Aware of various front panel controls and indicators.
- Connect and manipulate nodes and wires in the block diagram.
- Locate various tool bars and pull-down menus for the purpose of implementing specific functions.
- Locate and utilize the context help window.
- Familiar with LabVIEW and different applications using it.

Sl. No	**Experiments**
1	Basic arithmetic operations: addition, subtraction, multiplication and division
2	Boolean operations: AND, OR, NOT, XOR, NAND and NOR
3	Sum of ‘n’ numbers using ‘for’ loop and while loop
4	Factorial of a given number using ‘for’ loop and ‘while’ loop
5	Sorting even numbers using ‘while’ loop in an array
6	Simulation of Amplitude Modulation and Frequency modulation using LabVIEW.
7	Simulation of Binary Phase Shift Keying (BPSK) and Quadrature Phase Shift Keying (QPSK) Using LabVIEW.
8	Study of Signal Sampling and Reconstruction Using LabVIEW.
9	Build a Virtual Instrument that simulates a heating and cooling system. The system must be able to be controlled manually or automatically.
10	Build a Virtual Instrument that simulates a Basic Calculator (using formula node).
11	Build a Virtual Instrument that simulates a Water Level Detector.
12	Demonstrate how to create a basic VI which calculates the area and perimeter of a circle.
Demonstration Experiments	
13	Creation of a CRO using LabVIEW and measurement of frequency and amplitude from external source.

14	Create function generator using LabVIEW and display the amplitude and frequency on CRO (externally connected).
15	Demonstrate binary to grey code converter (&vice-versa) using DAQ card.

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Apply the fundamentals of graphical programming by creating Virtual Instruments (VIs) using front panel controls, indicators, and block diagrams.
CO2	Develop LabVIEW programs using programming structures such as loops, arrays, Boolean operations, and formula nodes to solve engineering problems.
CO3	Simulate basic communication and signal processing systems, including modulation techniques and signal sampling, using LabVIEW.
CO4	Design and implement virtual instrumentation applications for real-world engineering systems such as water level monitoring, heating and cooling control, and basic measurement systems.
CO5	Analyze, test, and validate the performance of virtual instruments by integrating signal generation, visualization, and data acquisition concepts

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	20	-	Marks awarded for Weekly Conduction of Experiments and Submission of Laboratory records, scaled to 20 marks.
CIE Practical Test + Mini Project (B)	10 + 20	-	Test conducted for part A and part B, each carries 5 marks and final IA test conducted for 20 Marks
Total CIE (A+B)	**50**	**20**	**Sum of Marks of Experiments, Record and Test shall be CIE marks awarded for a maximum of 50.**
SEE (C)	**50**	**20**	**SEE is a lab exam conducted for 100 marks and scaled down to 50 marks. Exam duration shall be for 3 hours.**
CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

Text Books:

1.	Jennings, Richard and De la Cueva, Fabiola, "LABVIEW Graphical Programming" (5th Edition) McGraw Hill, 2019
2.	Jovitha Jerome, "Virtual Instrumentation using LABVIEW", PHI, 2011
3.	Sanjay Gupta, Joseph John, "Virtual Instrumentation using LABVIEW", TMH, McGraw Hill, Second Edition,2011.

ESTD : 2001
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B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – IV			
Course Title	**Biology for Engineers**		
Course Code	**25BFETH407**	**CIE Marks**	**50**
(L: T: P) + SL	**(30: 0: 0) + 30 Hours / Sem**	**SEE Marks**	**50**
Credits	**2**	**Exam Hours**	**2**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Familiarize the students with the basic biological concepts and their engineering applications.
- Enable the students with an understanding of biodesign principles to create novel devices and structures.
- Provide the students an appreciation of how biological systems can be re-designed as substitute products for natural systems.
- Motivate the students to develop an interdisciplinary vision of biological engineering.

Module-1	**Introduction to fundamentals of life**	**6 hrs**
Structure and functions of a cell, Biomolecules: Properties and functions of Carbohydrates, Nucleic acids, Proteins, Enzymes and Lipids		
Module-2	**Introduction to applications of biomolecules**	**6 hrs**
Carbohydrates in cellulose-based water filters production, PHA and PLA in bioplastics, Nucleic acids in vaccines and diagnosis, Proteins in food production, Enzymes in biosensors fabrication, Genome & protein data types		
Module-3	**Introduction to adaptations of anatomical principles for bioengineering design**	**6 hrs**
Brain as a CPU system. Eye as a Camera system. Heart as a pump system. Lungs as a purification system. Kidney as a filtration system		
Module-4	**Introduction to nature inspired biomaterials and mechanisms**	**6 hrs**
Echolocation, Photosynthesis, Bird flying, Lotus leaf effect, Shark skin, Kingfisher beak. Artificial blood - haemoglobin-based oxygen carriers (HBOCs)		
Module-5	**Introduction to trends in bioengineering**	**6 hrs**
Bioprinting techniques and materials. Electrical tongue and electrical nose in food science, DNA origami and Biocomputing, Bioimaging and Artificial Intelligence for disease diagnosis. Bio concrete		

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Corroborate the concepts of biomimetics for specific requirements.
CO2	Understand the basic biological concepts for relevant industrial applications and adaptations.
CO3	Evaluate the principles of design and development for exploring engineering knowledge in the biological stream.
CO4	Explore innovative biobased solutions for socially relevant problems.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	30	-	Average of Two Internal Assessment Tests (MCQs) each conducted for 30 marks.
Continuous and Comprehensive Evaluation (B)	20	-	Any two Assessment methods as per 24RNBE4.2 scaled to 20 marks.
Total CIE (A+B)	**50**	**20**	**CIE Evaluation is done for a maximum of 50 marks**
SEE (C)	**50**	**18**	**Question Paper having 50 MCQs with each question carrying 01 mark, and exam duration shall be for 2 hours.**
CIE + SEE (A+B+C)	**100**	**40**	Final marks shall be the sum of marks scored in Components **A, B and C.**
• The minimum marks to be secured in CIE is 20 (40%) out of allotted 50 marks to appear for SEE.			

Text Books:

1.	Basuchandra's Biology for Engineers, Chandra Shekara. B.M, Basavaraju B.C, 2025.
2.	Biology for Engineers, Rajendra Singh C and Rathnakar Rao N, Rajendra Singh C and Rathnakar Rao N Publishing, Bengaluru, 2023.

Reference Books:

1.	Human Physiology, Stuart Fox, Krista Rompolski, McGraw-Hill eBook. 16th Edition, 2022 Biology for Engineers, Thyagarajan S., Selvamurugan N., Rajesh M.P., Nazeer R.A., Thilagaraj W. Barathi S., and Jaganthan M.K., Tata McGraw-Hill, New Delhi, 2012. Biology for Engineers, Arthur T. Johnson, CRC Press, Taylor and Francis, 2011 Biomedical Instrumentation, Leslie Cromwell, Prentice Hall 2011. Biology for Engineers, Sohini Singh and Tanu Allen, Vayu Education of India, New Delhi, 2014. Biomimetics: Nature-Based Innovation, Yoseph Bar-Cohen, 1st edition, 2012, CRC Press. Bio-Inspired Artificial Intelligence: Theories, Methods and Technologies, D. Floreano and C. Mattiussi, MIT Press, 2008. Bioremediation of heavy metals: bacterial participation, by C R Sunil kumar, N Geetha, A C Udaya shankar, Lambert Academic Publishing, 2019.

ESTD : 2001
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B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – IV			
Course Title	**NSS-National Service Scheme**		
Course Code	**25BNSSP409**	**CIE Marks**	**100**
(L: T: P) + SL	**(0: 0: 0) + 30 Hrs/sem**	**SEE Marks**	**-**
Credits	**-**	**Exam Hours**	**-**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Understand the community in general in which they work.
- Identify the needs and problems of the community and involve them in problem –solving.
- Develop among themselves a sense of social & civic responsibility & utilize their knowledge in finding practical solutions to individual and community problems.
- Develop competence required for group-living and sharing of responsibilities and gain skilling mobilizing community participation to acquire leadership qualities and democratic attitudes.
- Develop capacity to meet emergencies and natural disasters & practice national integration and social harmony in general.

Module 1		**6 hrs**
Water conservation techniques – Role of different stakeholders– Implementation.		
Module 2		**6 hrs**
Preparing an actionable business proposal for enhancing the village income and approach for implementation.		
Module 3		**6 hrs**
Helping local schools to achieve good results and enhance their enrolment in Higher/technical/ vocational education.		
Module 4		**6 hrs**
NSS Activities -1		
Module 5		**6 hrs**
NSS Activities -2		

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Understand the significance of individual responsibilities towards society and contribute meaningfully to community welfare.
CO2	Analyze environmental and societal issues, and design feasible solutions to address them effectively
CO3	Critically evaluate existing systems and propose practical, sustainable solutions for long-term development.
CO4	Plan and implement government initiatives or self-driven projects effectively in real-life community settings.
CO5	Develop the capacity to respond to emergencies and natural disasters, while practicing national integration, social harmony, and unity in diversity.

Activity list:

Sl. No	Activity	Deliverables
1	Plantation Drive: Adopt a Tree	Developing and managing an efficient garbage disposal system
2	Food Preservation/ Packaging awareness	Tourism Promotion: Innovative Approaches
3	Facilitating 100% digitized money transactions	Contribution to any national-level initiative of the Government of India. E.g. Digital India/ Skill India/ Swachh Bharat Internship etc.,

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	60	-	Sum of Two Internal Assessment Tests (MCQs) each conducted for 30 marks.
Continuous and Comprehensive Evaluation (B)	40	-	Any two assessment methods as per 24RNBE4.2, scaled to 40 marks.
CIE + SEE (A+B)	**100**	**40**	CIE Evaluation is done for a maximum of 100 marks
• The minimum marks to be secured in CIE is 40 (40%) out of 100 marks allotted to Pass.			

Text Books:

1.	NSS Course Manual, Published by NSS Cell, VTU Belagavi.
2.	Government of Karnataka, NSS cell, activities reports and its manual.
3.	Government of India, NSS cell, Activities reports and its manual.

Web links:

1.	https://nss.gov.in/
2.	https://pledge.mygov.in/

ESTD : 2001
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B.E. (Electronics and Communication Engineering)
Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
SEMESTER – IV

Course Title	**Physical Education**		
Course Code	**25BPEDU409**	**CIE Marks**	**100**
(L: T: P) + SL	**(0: 0: 0) + 30 Hrs / sem**	**SEE Marks**	**-**
Credits	**-**	**Exam Hours**	**-**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Understand the fundamental concepts of Physical Education, games and sports skills, Health, Nutrition and Fitness
- Familiarization of health-related Exercises, Sports for overall growth and development
- Participate in the competition at regional/state / national / international levels.
- Create consciousness among the students on Health, Fitness and Wellness in developing and maintaining a healthy lifestyle.

Module 1		**6 hrs**

Athletics

- Track - Sprints
- Throws - Shotput
- Jumps - Long jump
- **Track Events**
- Starting Techniques: Standing start and Crouch start (its variations) use of Starting Block.
- Acceleration with proper running techniques.
- Finishing technique: Run Through, Forward Lunging and Shoulder Shrug, Torso Finish.

B. Long Jump

Approach Run, Take-off, Flight in the air (Hang Style/Hitch Kick) and Landing

C. Shot put

Holding the Shot, Placement, Initial Stance, Glide, Delivery Stance and Recovery (Perry O'Brien Technique)

Module 2		**6 hrs**

Volleyball

A. Fundamental skills

1. Service: Underarm Service, Side arm Service, Tennis Service, Floating Service
2. Pass: Under arm Pass, Overhead Pass
3. Spiking & Blocking
4. Game Practice with application of Rules & Regulations

B. Rules and their interpretation and duties of the officials

Module 3		6 hrs
Throwball **A. Fundamental skills** Overhand service, Side arm service, two hand catching, one hand overhead return, side arm return. **B. Rules and their interpretation and duties of the officials**		

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Understand the fundamental concepts of Physical Education, games and sports skills, Health, Nutrition and Fitness
CO2	Familiarization of health-related Exercises, Sports for overall growth and development
CO3	Participate in the competition at regional/state/national/international levels.
CO4	Create consciousness among the students on Health, Fitness and Wellness in developing and maintaining a healthy lifestyle.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE Theory (A)	60	-	Sum of Two Internal Assessment Tests (MCQs) each conducted for 30 marks.
QUIZ (B)	40	-	Quiz for a maximum of 40 marks
TOTAL CIE (A+B)	100	40	**CIE Evaluation is done for a maximum of 100 marks**
• The minimum marks to be secured in CIE is 40 out of allotted 50 marks with minimum 40 % scored in every component of CIE.			

Text Books:

1.	Saha, A. K. Sarir Siksher Ritiniti, Rana Publishing House, Kalyani.
2.	Bandopadhyay, K. Sarir Siksha Parichay, Classic Publishers, Kolkata.

Reference Books:

1.	Saraswati Health and Physical Education Textbook
2.	V.K. Sharma's Health and Physical Education

B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – III			
Course Title	**Yoga**		
Course Code	**25BYOGA409**	**CIE Marks**	**100**
(L: T: P) + SL	**(0: 0: 0) + 30 Hrs / sem**	**SEE Marks**	**-**
Credits	**-**	**Exam Hours**	**-**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Physical, Mental & spiritual Objectives of Yoga
- Explain the meaning of Yoga.
- Discuss the importance of the Yoga and its scope.
- Describe the aims and objectives of Yoga.
- Clarify the misconceptions on Yoga

Module 1		**6 hrs**

Patanjali Ashtanga Yoga

A. Yama: Ahimsa, satya, asteya, brahmacarya, aparigraha

B. Niyama: shoucha, santosh, tapa, svaadhyaya, Eshvarapranidhan

C. Suryanamaskara: 12 Counts, 4 Rounds

Module 2		**6 hrs**

Asana

- Meaning, Need & Importance of Asana
- **Different Types of Asanas:**
  1. **Sitting** - 1. Sukhasana, 2. Paschimottanasana
  2. **Standing** - 1. ArdhakatiChakrasana 2. Parshva Chakrasana
  3. **Prone line** - Dhanurasana
  4. **Supine line-** Halasana
- Asana Technique
- Precautionary measures and benefits of each Asana

Module 3		**6 hrs**

Pranayama

- Meaning, Need & importance of Pranayama.

  Different types of pranayama, technique, precautionary measures and benefits of each Pranayama.

  1. **Suryanuloma -Viloma**
  2. **Chandranu loma-Viloma**
- **Kapalabhati**

  Meaning, importance and benefits of Kapalabhati.

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Understand the fundamental concepts of Yoga
CO2	Improves of health and related aspects, overall growth and development
CO3	Participate in the competition at regional/state/national/international levels.
CO4	Create consciousness among the students on Health, Fitness and Wellness in developing and maintaining a healthy lifestyle.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE Theory (A)	60	-	Sum of Two Internal Assessment Tests (MCQs) each conducted for 30 marks.
QUIZ (B)	40	-	Quiz for a maximum of 40 marks
TOTAL CIE (A+B)	100	40	**CIE Evaluation is done for a maximum of 100 marks**
• The minimum marks to be secured in CIE is 40 out of allotted 50 marks with minimum 40 % scored in every component of CIE.			

Text Books:

1.	The Yoga Sutras of Patanjali – Sri Swami Satchidananda.
2.	Light on Yoga — B.K.S Iyengar.

Reference Books:

1.	The Heart of Yoga — T.K.V Desikachar.
2.	“Asana Pranayama Mudra Bandha” by Swami Satyananda Saraswati.

B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – IV			
Course Title	**Music**		
Course Code	**25BMUSK409**	**CIE Marks**	**100**
(L: T: P) + SL	**(0: 0: 0) + 30 Hrs/sem**	**SEE Marks**	**-**
Credits	**-**	**Exam Hours**	**-**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Understand the significance of music in daily life and gain an overview of Indian folk, contemporary, and Western music traditions.
- Acquire basic knowledge of introductory Carnatic music exercises and compositions.
- Compare the fundamental features of Carnatic and Hindustani music.
- Recognize the classification of wind instruments and appreciate the contributions of eminent composers to Indian classical music.

Module 1		**6 hrs**
Importance of music in daily life, Indian folk, and contemporary music. Introduction to Western music		
Module 2		**6 hrs**
Compositions: Introduction to the few types of composition in Carnatic Music- Nottu Swara, Sarale and Janti varase, Alankara		
Module 3		**6 hrs**
Comparative Study of Carnatic and Hindustani Music based on Geographical origin and development, Musical structure and style, Raga and Tala systems		
Module 4		**6 hrs**
Music Instruments: Classification and construction of wind instruments in both Carnatic and Hindustani Music.		
Module 5		**6 hrs**
Composers: Biography and contributions of the following eminent personalities Muttuswami Dikshitar, Shyama Shastri, Mysore Vasudevacharya, Pt. Bhimsen Joshi		

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Explain the importance of music in daily life and the characteristics of Indian folk, contemporary, and Western music traditions.

CO2	Illustrate the basic concepts and structure of introductory Carnatic music exercises and compositions.
CO3	Compare the distinguishing features of Carnatic and Hindustani music.
CO4	Analyze the contributions of eminent composers in enriching and preserving the heritage of Indian classical music.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	60	-	Sum of Two Internal Assessment Tests (MCQs) each conducted for 30 marks.
Continuous and Comprehensive Evaluation (B)	40	-	Any two assessment methods as per 24RNBE4.2, scaled to 40 marks.
CIE + SEE (A+B)	**100**	**40**	CIE Evaluation is done for a maximum of 100 marks
• The minimum marks to be secured in CIE is 40 (40%) out of 100 marks allotted to Pass.			

Text Books:

1.	Vidushi Vasantha Madhavi, “Theory of Music”, Prism Publication, 2007.
2.	T Sachidevi and T Sharadha (Thirumalai Sisters), Karnataka Sangeetha Dharpana- Vol. 1 (English), Shreenivaas Prakaashana, 2018.
3.	B. Chaitanya Deva, An Introduction to Indian Music, Publications Division, Government of India, New Delhi.

Reference Books:

1.	Lakshminarayana Subramaniam, Viji Subramanaim, "Classical Music of India: A Practical Guige, Tranqueber 2018.
2.	R. Rangaramanuja Ayyangar, "History of South Indian (Carnatic) Music", Vipanci Charitable Trust; Third edition, 2019,
3.	Vamanrao H. Deshpande, Indian Musical Traditions: An Aesthetic Study of the Gharanas in Hindustani Music, Popular Prakashan, Mumbai.

B.E. (Electronics and Communication Engineering) Outcome Based Education (OBE) and Choice Based Credit System (CBCS) SEMESTER – IV			
Course Title	**Mathematics course for Lateral Entry Students**		
Course Code	**25BMADP410**	**CIE Marks**	**100**
(L: T: P) + SL	**(14: 0: 0) + 14 Hours / Sem**	**SEE Marks**	**-**
Credits	**-**	**Exam Hours**	**-**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

- Apply the essential concepts of linear algebra to solve systems of linear equations and analyze mathematical models.
- Solve second- and higher-order ordinary differential equations using appropriate analytical methods in engineering contexts.
- Develop the knowledge and problem-solving skills required to evaluate multiple integrals, apply change of order of integration.
- Apply numerical methods to obtain approximate solutions to mathematical problems arising in science and engineering.

Module 1	**Linear Algebra**	**3 hrs**
Introduction - rank of matrix by elementary row operations - Echelon form. Consistency of system of linear equations - Gauss elimination method. Eigen values and Eigen vectors of a square matrix. Problems.		
Module 2	**Numerical Methods**	**3 hrs**
Finite differences. Interpolation/extrapolation using Newton's forward and backward difference formulae (Statements only)-problems. Solution of polynomial and transcendental equations – Newton-Raphson and Regula-Falsi methods (only formulae)- Illustrative examples. Numerical integration: Simpson's one third rule (without proof) Problems.		
Module 3	**Higher order ODE's**	**3 hrs**
Linear differential equations of second and higher order equations with constant coefficients. Homogeneous /non-homogeneous equations. Inverse differential operators. *[Particular Integral restricted to* $R(x)=e^{ax}$, $\sin ax$ /$\cos ax$ *for* $f(D)y = R(x)$.]		
Module 4	**Double integrals**	**3 hrs**
Definition, evaluation of rectangular and general regions, Change of order of integration.		
Module 5	**Triple integrals**	**2 hrs**
Definition and evaluation over simple regions, Applications of triple integrals to the evaluation of volumes.		

Course Outcomes:

After successfully completing the course, the student will be able to:

CO1	Solve systems of linear equations using matrix algebra.
CO2	Apply the knowledge of numerical methods in modelling and solving engineering problems. CO3: Apply analytical methods to solve higher order differential equations.
CO3	Solve double integrals, including change of order of integration,
CO4	Solve triple integrals, volumes of geometrical regions.
CO5	Solve systems of linear equations using matrix algebra.

Assessment Details (CIE and SEE):

Assessment Type	Maximum Marks	Minimum Passing Marks	Evaluation Details
CIE – IA Tests (A)	60	-	Sum of Two Internal Assessment Tests (MCQs) each conducted for 30 marks.
Continuous and Comprehensive Evaluation (B)	40	-	Any two assessment methods as per 24RNBE4.2, scaled to 40 marks.
CIE + SEE (A+B)	**100**	**40**	CIE Evaluation is done for a maximum of 100 marks
• The minimum marks to be secured in CIE is 40 (40%) out of 100 marks allotted to Pass.			

Text Books:

1.	B. S. Grewal, "Higher Engineering Mathematics", Khanna Publishers, 43rd Edition, 2015.

Reference Books:

1.	E. Kreyszig, "Advanced Engineering Mathematics", John Wiley & Sons, 10th Edition, 2015
2.	N. P. Bali, Manish Goyal, "Engineering Mathematics", Laxmi Publishers, 7th Edition, 2007
3.	Rohit Khurana, "Engineering Mathematics", Vol. I, Cengage Learning, 1st Edition, 2015

Additional Mathematics I and II:

- These courses are prescribed for III and IV semesters respectively to lateral entry Diploma holders admitted to III semester of B.E./B.Tech., programs. They shall attend the classes during the respective semesters to complete all the formalities of the course and appear for the Continuous Internal Evaluation (CIE). In case any student fails to register for the said course/fails to secure the minimum 40 % of the prescribed CIE marks, he/she shall be deemed to have secured an F grade. In such a case, the student has to fulfill the course requirements during subsequent semesters to earn the qualifying CIE marks. These courses are slated for CIE only and have no SEE.
- Additional Mathematics I and II shall not be considered for vertical progression as well as for the calculation of SGPA and CGPA, but completion of the courses shall be mandatory for the award of degree.
- Successful completion of the courses Additional Mathematics I and II shall be indicated as satisfactory in the grade card. Non-completion of the courses Additional Mathematics I and II shall be indicated as Unsatisfactory.

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Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
Skill Development Course
SEMESTER-IV

Course Title:	**VLSI and Embedded System**		
Course Code:	**25BECSL001**	**CIE MARKS**	**50**
L : T : P + (SL)	**0:0:30**	**SEE MARKS**	**50**
Credits:	**1**	**EXAM HOURS**	**3**

COURSE LEARNING OBJECTIVES: *The purpose of the course is to facilitate the learner to:*

- Explain the fundamentals of finite state machines and develop behavioural Verilog code to implement sequential digital systems using Vivado and Artix-7 FPGA.
- Design, simulate, and synthesize FSM-based applications using Verilog HDL.
- Design and study CMOS circuits, such as inverters, buffers, pass-transistor logic, and transmission gates, using Cadence tools.
- Analyse CMOS circuit performance by studying delay, power consumption, transistor sizing, voltage transfer characteristics, and MOSFET behaviour.
- Apply VLSI and digital design concepts to build practical projects involving FSMs, CMOS circuits, current mirrors, and current multipliers.

Sl no	Experiments / Hands-on learning
1.	Implementation of coffee vending machine/
2.	Implementation of coin phone booth
3.	Implementation of sequence detector.
4.	Implementation of Tea vending machine.
5.	Implementation of digital stop watch.
6.	Implementation of Pizza vending machine.
7.	Implementation of Pseudorandom sequence generator.
8.	Implementation of calculator.
9.	Implementation of Exam process.
10.	Implementation of Library book borrowing system.
11.	Implementation of Smart call handling system.
12.	Implementation of Online shopping system.
13.	Implementation of Airport Check in process.
14.	Implementation of Smart home thermostat.
15.	Implementation of ATM system.
16.	Implementation of Media player.
17.	Implementation of Login authentication flow.
18.	Implementation of Washing machine.
19.	Implementation of Rock, Paper, Scissor board game.
20.	Implementation of Chat bot conversation flow.
21.	Implementation of smart helmet for drowsiness detection, unauthorized access to vehicle
22.	Implementation of smart walking stick to guide a blind person
23.	Implementation of smart watch to monitor the vitals of patient.
24.	Implementation of smart cradle to monitor the babies sleep and prevent from falling.

25.	CMOS Inverter Design and Transistor Sizing Design a CMOS inverter and vary the PMOS-to-NMOS width ratio. • Plot the voltage transfer characteristic (VTC). • Measure switching threshold and noise margins. • Compare rise time, fall time and propagation delay. Deliverable: Graphs showing how transistor sizing affects inverter
26.	Design of a CMOS Buffer for a Large Capacitive Load Design a chain of inverters to drive a large load capacitance. • Compare a single inverter with a multistage buffer. • Vary the size ratio between successive stages. • Measure delay, power and area. Deliverable: The buffer sizing strategy that gives the best delay under an area or power constraint
27.	MOSFET I–V Characteristic Analyzer Simulate an NMOS and PMOS and study their drain-current characteristics. • Sweep VGS and plot ID versus VDS. • Repeat for different gate voltages. • Identify cut-off, linear and saturation regions. • Extract threshold voltage and trans-conductance. Outcome: MOSFET I–V curves and extracted device parameters.
28.	NMOS/PMOS Pass Transistor and the Weak Logic-1/Weak Logic-0 Problem Use a single NMOS transistor as a switch to transfer a digital input. • Apply logic 0 and logic 1 at the input. • Measure the output voltage. • Observe why a high output may be limited under simple operating assumptions. • Investigate the effect of body effect and supply voltage. Outcome: Demonstrate the voltage degradation associated with an NMOS pass transistor.
29.	Design and Analysis of a Pass-Transistor XOR Gate Implement an XOR gate using pass-transistor logic and compare it with a conventional CMOS implementation. • Verify the truth table. • Measure output-high and output-low levels. • 30Compare transistor count, propagation delay and power. • Check whether output restoration is required. Outcome: Understand the area and performance trade-offs of pass-transistor logic.
30.	Effect of Cascaded Pass Transistors on Logic Levels Connect multiple pass transistors in a chain and study signal degradation. • Measure output voltage after each stage. • Compare different transistor sizes. • Investigate the effect of load capacitance. • Propose a buffer or level-restoration solution. Outcome: Identify limitations when pass-transistor stages are cascaded.
31.	Design of a 2:1 Multiplexer Using Transmission Gates Implement a multiplexer using two transmission gates and an inverter for select control. • Verify all input/select combinations. • Measure propagation delay. • Compare transistor count and power with a conventional CMOS mux.

	• Investigate the effect of output load capacitance. Outcome: A functional transmission-gate multiplexer with performance measurements.
32.	Transmission-Gate Latch Build a level-sensitive latch using transmission gates and inverters. • Verify transparent and hold modes. • Study timing behaviour with a clock. • Measure propagation delay and setup/hold behaviour where applicable. • Examine how transistor sizing affects delay and power. Outcome: Understand how transmission gates are used in sequential CMOS circuits.
33.	Transmission-Gate D-Flipflop Build a Edge Sensitive-sensitive latch using transmission gates and inverters
34.	Design and Simulation of a CMOS Ring Oscillator
35.	Design and Characterization of a Basic CMOS Current Mirror Design a two-transistor NMOS current mirror and verify how accurately it copies a reference current. • Sweep the output voltage and plot output current. • Determine the minimum output voltage required for proper operation. • Measure current-mirror error and output resistance. • Study the effect of transistor sizing. Deliverable: Output-current-versus-output-voltage graph and current-mirror accuracy analysis.
36.	Design of a CMOS Current Multiplier Beginner Use transistor sizing ratios to generate an output current that is a multiple of the reference current. • Design ×1, ×2 and ×4 current outputs.
Demonstration Experiments (For CIE)	
1.	Introduction to State machines, Introduction to Behavioural style Verilog code.
2.	Implementation of traffic light system.
3.	Implementation of seat belt warning system
4.	Demonstration of drone Flight control system.
5.	Introduction to CMOS logic circuits, Transistor sizing in CMOS circuits, Effect of sizing on circuit performance, Hands on with small examples.
6.	Propagation delay in CMOS circuits, Factors affecting delay, Power calculation in CMOS circuits, hands on of Delay and power analysis.
7.	Characterization of MOSFET using parametric analysis, Pass transistors and Transmission Gate, DC characteristics of Ratioed and Ratioless logic circuit.
8.	Current mirrors and current multipliers(steering circuits)

COURSE OUTCOMES:

After successfully completing the course, the student will be able to:

CO1	Develop finite state machines using behavioural Verilog HDL for implementing sequential digital systems..
CO2	Simulate and synthesize FSM-based applications using Vivado and demonstrate their functionality on FPGA platforms.
CO3	Design and simulate CMOS logic circuits using Cadence tools, considering transistor sizing

	and circuit characteristics..
CO4	Analyse CMOS circuit performance in terms of propagation delay, power consumption, MOSFET characteristics, and logic-level behaviour.
CO5	Implement practical VLSI and digital system design projects using Verilog HDL and CMOS circuit design techniques.

Suggested Learning Resources:

1. Vivado Design Suite – User Guides and Tutorials.
For creating Verilog projects, running simulation, synthesis, implementation, and FPGA programming.
https://www.amd.com/en/developer/resources/vivado.html?utm_source=chatgpt.com

2. Embedded Design Tutorial (PDF/manual)
Official guide to embedded hardware design using Vivado and related tools.
https://docs.amd.com/r/2022.1-English/ug940-vivado-tutorial-embedded-design?utm_source=chatgpt.com

3. Cadence Academic Resources
Academic learning resources for circuit design, schematic entry, simulation, and IC design.

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B.E. (Electronics and Communication Engineering)
Outcome Based Education (OBE) and Choice Based Credit System (CBCS)
Skill Development Course
SEMESTER-IV

Course Title	**Signal Processing Applications with AI**		
Course Code	**25BECSL002**	**CIE Marks**	**50**
(L: T: P) + SL	**(0: 0: 30)**	**SEE Marks**	**50**
Credits	**1**	**Exam Hours**	**3**

Course Learning Objectives:

The purpose of the course is to facilitate the learner to:

Understand core signal-processing concepts and how MATLAB represents and analyse signals.
Use Signal Processing Toolbox functions to filter signals and design, analyse, and apply digital filters.
Perform frequency-domain analysis using Fourier transforms and spectral estimation.
Analyze signals in time and frequency domains using appropriate methods and visualizations.
Apply toolbox workflows to common tasks such as noise reduction, feature extraction, and signal measurement.

Module-1	**Signal Generation, Analysis, and Pre-processing**	**2 hrs**
Process a Signal with Missing Samples, Measure Signal Similarities, Align Signals with Different Start Times, Resample Uniformly and Non-uniformly Sampled Signals, Find a Signal in a Measurement.		
Module-2	**Waveform Generation, Signal Analysis and Visualization**	**2 hrs**
Compute Envelope Spectrum of Vibration Signal, **Experiment 1**: Extract Voices from Music Signal, **Experiment 2:** Extract Regions of Interest from Whale Song.		
Module-3	**Smoothing and Denoising**	**2 hrs**
Signal Smoothing, Remove Trends from Data, Remove the 60 Hz Hum from a Signal, Remove Spikes from a Signal, and Reconstruct a Signal from Irregularly Sampled Data.		
Module-4	**Measurements and Feature Extraction**	**2 hrs**
Distortion Measurements, Determine Peak Widths, **Experiment 3:** Classify ECG Signals Using Long Short-Term Memory Networks, **Experiment 4:** Human Activity Recognition Using Signal Feature Extraction and Machine Learning, **Experiment 5:** Waveform Segmentation Using Deep Learning.		
Module-5	**Descriptive Statistics**	**2 hrs**
Measure Signal Similarities, Extract Classification Features from Physiological Signals, Automate Signal Labelling with Custom Functions. **Capstone Project:** Human Activity Recognition Simulink Model for Smartphone Deployment.		
Module-6	**Transforms, Correlation, and Modelling**	
Single Sideband Modulation Using Hilbert Transform, DCT for Speech Signal Compression, Walsh-Hadamard Transform for Spectral Analysis and Compression of ECG Signals		

Module-7	**Time-Frequency Analysis**	
Waveform Segmentation Using Deep Learning, Spectral Descriptors. **Capstone Project** : Spoken Digit Recognition with Custom Log Spectrogram Layer and Deep Learning		
Module-8	**Vibration Analysis**	
Compute Envelope Spectrum of Vibration Signal, Vibration Analysis of Rotating Machinery. **Capstone Project:** Machine Learning and Deep Learning Classification Using Signal Feature Extraction Objects		
Module-9	**AI for Signals - I**	**2 Hrs**
CBRS Band Radar Detection in 5G Signals and Noise Using YOLOX. **Capstone Project** :Hand Gesture Classification Using Radar Signals and Deep Learning		
Module-10	**AI for Signals - II**	**2 Hrs**
Musical Instrument Classification with Joint Time-Frequency Scattering, Classify Arm Motions Using EMG Signals and Deep Learning, **Capstone Project** : Pedestrian and Bicyclist Classification Using Deep Learning		

COURSE OUTCOMES: After successfully completing the course, the student will be able to:	
CO1	Import, generate, and visualize signals in MATLAB using Signal Processing Toolbox functions.
CO2	Process noisy signals using appropriate filtering and noise-reduction techniques
CO3	Select suitable Signal Processing toolbox functions and AI workflows for signal-processing tasks.
CO4	Develop MATLAB scripts or live scripts to perform signal analysis and processing.
CO5	Evaluate and validate results using relevant plots, measurements, and performance criteria.

Suggested Learning Resources:

4. Signal Processing Toolbox Getting Started Guide
   (https://in.mathworks.com/help/releases/R2026b/pdf_doc/signal/signal_gs.pdf)
5. Signal Processing Toolbox User's Guide
   (https://in.mathworks.com/help/releases/R2026b/pdf_doc/signal/signal.pdf)
6. Signal Processing Toolbox Reference
   (https://in.mathworks.com/help/releases/R2026b/pdf_doc/signal/signal_ref.pdf)



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Building RNSIT into a World Class Institution.

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- Imparting value based, need based, choice based and skill based professional education to the aspiring youth and carving them into disciplined, World class professionals with social responsibility.
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